RS5C317A/B

OUTLINE

The RS5C317A/B are CMOS type real-time clock ICs which are connected to the CPU via three signal lines and capable of serial transmission of clock and calendar data to the CPU. The RS5C317A/B can generate various periodic interrupt clock pulses lasting for long period (one month), further alarm interrupt can be made by days of the week, hours, and minutes. The function of 32kHz clock output and timer counter for watch-dog-timer are also include. Driving an oscillation circuit at constant voltage, the circuit undergoes few voltage fluctuations and consequently realizes low current consumption (0.6µA at 3V). It also provides an oscillator halt sensing function for application to data validity at power-on and other occasions. Integrated into a compact and thin 14pin SSOP (0.65mm pitch), the RS5C317A/B are the optimum choice for equipment requiring small size and low power consumption.

The RS5C317A and the RS5C317B reads/writes data at falling and rising edge of serial clock respectively.

FEATURES

- Time keeping voltage 1.6V to 6.0V
- Lowest supply current 0.6µA TYP. (1.5µA MAX.) at 3V
- Connection to the CPU via only three pins: CE, SCLK/SCLK and SIO for addressing and data read/write
- A clock counter (counting hours, minutes, and seconds) and a calendar counter (counting leap years, years, months, days, and days of the week) in BCD code
- Periodic interrupt pulses to the CPU with cycles ranging from one month to 1/1024Hz, with interrupt flags and interrupt halt
- Alarm interrupt (days of the week, hours, minutes)
- Counter for timer with internal clock
- Oscillator halt sensing to judge internal data validity
- 32kHz clock output with enable switch
- Second digit adjustment by ±30 seconds
- 12-hour or 24-hour time display selectable
- Automatic leap year recognition up to the year 2099
- CMOS logic
- Package: 14pin SSOP (0.65mm pitch)
APPLICATIONS

- Communication equipment (Multi-function telephone, portable telephone, PHS, pager)
- Business machine (Facsimile, portable facsimile)
- Personal computer (Desktop type, notebook type, word processor, PDA, electronic notebook, TV games)
- Audio visual equipment (Portable audio equipment, video camera, camera, digital camera, remote control equipment)
- Home use (Rice cooker, microwave range)

PIN CONFIGURATION

- 14pin SSOP (0.65mm pitch)

<table>
<thead>
<tr>
<th></th>
<th>RS5C317A</th>
<th>RS5C317B</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SCLK</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>SIO</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>CLKC</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>ALRM</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>TMOUT</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>VSS</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>14 VDD</td>
<td>14 VDD</td>
</tr>
<tr>
<td></td>
<td>13 32KOUT</td>
<td>13 32KOUT</td>
</tr>
<tr>
<td></td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td></td>
<td>OSCIN</td>
<td>OSCIN</td>
</tr>
<tr>
<td></td>
<td>OSCOUT</td>
<td>OSCOUT</td>
</tr>
<tr>
<td></td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td></td>
<td>INTR</td>
<td>INTR</td>
</tr>
</tbody>
</table>
# PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CE</td>
<td>Chip enable input</td>
<td>The CE pin is used to interface the CPU and is accessible when held at the high level. This pin is connected to a pull-down resistor. It should be switched to the low level or opened when not accessed or when powering off the system. Holding the CE pin high for more than 2.5 seconds forces 1Hz interrupt pulses to be output from the INTR pin for oscillation frequency measurement. (No “1Hz pulse” is output for less than 1.5 seconds.)</td>
</tr>
<tr>
<td>2</td>
<td>SCLK (A type)</td>
<td>Shift clock input</td>
<td>This pin is used to input shift clock pulses to synchronize data input to, and output from, the SIO pin. SCLK and ( \overline{SCLK} ) are for writing data at falling and rising edge of clock pulses respectively and also reading data at rising and falling edge of clock pulses respectively.</td>
</tr>
<tr>
<td>3</td>
<td>SIO</td>
<td>Serial input/output</td>
<td>The SIO pin inputs and outputs written or read data in synchronization with shift clock pulses from the SCLK/( \overline{SCLK} ) pin. The SIO pin causes high impedance when CE pin is held at the low level (CMOS input/output). After the CE pin is switched to the high level and the control bits and the address bits are input from the SIO, the SIO pin performs serial input and output operations.</td>
</tr>
<tr>
<td>8</td>
<td>INTR</td>
<td>Interrupt output</td>
<td>The INTR pin outputs periodic interrupt pulses and alarm interrupt to the CPU. This pin functions as an Nch open drain output even when the CE pin is held at the low level.</td>
</tr>
<tr>
<td>5</td>
<td>ALRM</td>
<td>Alarm output</td>
<td>The ALRM pin outputs alarm interrupt to the CPU. This pin functions as an Nch open drain output even when the CE pin is held at the low level.</td>
</tr>
<tr>
<td>6</td>
<td>TMOUT</td>
<td>Timer output</td>
<td>TMOUT pin outputs timer counter output pulses for watch-dog-timer and free-run-timer. This pin functions as an Nch open drain output even when the CE pin is held at the low level. Timer function is disabled and TMOUT is OFF state when the RS5C317 is in the oscillation halt sensing state.</td>
</tr>
<tr>
<td>11, 10</td>
<td>OSCIN, OSCOUT</td>
<td>Oscillator circuit input/output</td>
<td>These pins configure an oscillator circuit by connecting a 32.768kHz crystal oscillator between the OSCIN and OSCOUT pins and by connecting a capacitor between the OSCIN and Vss pins. (Any other oscillator circuit components are built into the RS5C317A/B.)</td>
</tr>
<tr>
<td>13</td>
<td>32KOUT</td>
<td>32kHz output</td>
<td>32kHz clock output pin for peripheral circuit. The 32kHz clock output is controlled by CLKC pin and 32kHz control register. The 32KOUT pin outputs 32kHz clock when the CLKC pin is held at high and CLEN=0, and this pin is held at high impedance state when the CLKC pin and CLEN is in any other states and even when the CLKC pin is open. CMOS output.</td>
</tr>
<tr>
<td>4</td>
<td>CLKC</td>
<td>Control input for 32kHz output</td>
<td>Control pin for an output of the 32KOUT pin. This pin incorporates a pull-down resistor.</td>
</tr>
<tr>
<td>14, 7</td>
<td>VDD, VSS</td>
<td>Positive/Negative power supply input</td>
<td>VDD and Vss is connected to power supply and ground respectively.</td>
</tr>
<tr>
<td>9, 12</td>
<td>NC</td>
<td>No Connection</td>
<td>Ordinarily connected to Vss pin.</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td></td>
<td>~0.3 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>Vt</td>
<td>Input voltage</td>
<td></td>
<td>~0.3 to VDD+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VO1</td>
<td>Output voltage 1</td>
<td>SIO, 32KOUT</td>
<td>~0.3 to VDD+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VO2</td>
<td>Output voltage 2</td>
<td>INTR, ALRM, TMOUT</td>
<td>~0.3 to +12</td>
<td>V</td>
</tr>
<tr>
<td>PD</td>
<td>Power dissipation</td>
<td>Topt=25°C</td>
<td>300</td>
<td>mW</td>
</tr>
<tr>
<td>Topt</td>
<td>Operating temperature</td>
<td></td>
<td>~40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage temperature</td>
<td></td>
<td>~55 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td></td>
<td>2.5</td>
<td>6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCLK</td>
<td>Time keeping voltage</td>
<td></td>
<td>1.6</td>
<td>6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>fXT</td>
<td>Oscillation frequency</td>
<td></td>
<td>32.768</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CG</td>
<td>External oscillation capacitance</td>
<td>Cl. value of crystal=6 to 8pF</td>
<td>5</td>
<td>10</td>
<td>24</td>
<td>pF</td>
</tr>
<tr>
<td>VPUP</td>
<td>Pull-up voltage</td>
<td>INTR, ALRM, TMOUT</td>
<td></td>
<td>10</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
**DC CHARACTERISTICS**

Unless otherwise specified: Vss=0V, Vdd=3V, T_0pt=-40 to +85˚C, Oscillation frequency=32.768kHz, (Cl=6pF, R1=30kΩ), Cg=10pF

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Pin name</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>“H” input voltage</td>
<td>CE, SCLK/SCLK, SIO, CLKC</td>
<td></td>
<td>0.8VDD</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>“L” input voltage</td>
<td>CE, SCLK/SCLK, SIO, CLKC</td>
<td></td>
<td>0</td>
<td>0.2VDD</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IOH</td>
<td>“H” output current</td>
<td>SIO, 32KOUT</td>
<td>VOH=VDD ~0.5V</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IOL1</td>
<td>“L” output current</td>
<td>SIO, 32KOUT</td>
<td>VOL1=0.5V</td>
<td>0.5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IOL2</td>
<td>“L” output current</td>
<td>INTR, ALARM, TMOUT</td>
<td>VOL2=0.4V</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RDN</td>
<td>Pull-down resistance</td>
<td>CE</td>
<td></td>
<td>45</td>
<td>150</td>
<td>450</td>
<td>kΩ</td>
</tr>
<tr>
<td>IIH</td>
<td>Input current</td>
<td>CLRC</td>
<td>VIH=3V</td>
<td>1</td>
<td>5</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>IIK</td>
<td>Input leakage current</td>
<td>SCLK/SCLK</td>
<td>Vi=VDD or Vss</td>
<td>~1</td>
<td>1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>IOZ1</td>
<td>Output leakage current</td>
<td>SIO, 32KOUT</td>
<td>Vo=VDD or Vss</td>
<td>~2</td>
<td>2</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>IOZ2</td>
<td>Output leakage current</td>
<td>INTR, ALARM, TMOUT</td>
<td>Vo=10V</td>
<td>~5</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IDD1</td>
<td>Standby current 1</td>
<td>VDD</td>
<td>VDD=3V</td>
<td>Input/output: open</td>
<td>0.6</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>IDD2</td>
<td>Standby current 2</td>
<td>VDD</td>
<td>VDD=6V</td>
<td>Input/output: open</td>
<td>0.8</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>Cd</td>
<td>Internal oscillation Cap.</td>
<td>OSCOUT</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

**AC CHARACTERISTICS**

(Vss=0V, T_0pt=-40 to +85˚C, Cl=50pF)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>VDD=4.5V</th>
<th>VDD=4.0V</th>
<th>VDD=2.5V</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCES</td>
<td>CE set-up time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCEH</td>
<td>CE hold time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCR</td>
<td>CE inactive time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSCK</td>
<td>SCLK clock cycle time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCKH</td>
<td>SCLK high time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCL</td>
<td>SCLK low time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCKS</td>
<td>SCLK to CE set-up time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tRE</td>
<td>Data output start time (from rising of SCLK) (from falling of SCLK)</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tRR</td>
<td>Data output delay time (from rising of SCLK) (from falling of SCLK)</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tRZ</td>
<td>Output floating time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDS</td>
<td>Input data set-up time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDH</td>
<td>Input data hold time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
TIMING CHARTS
Input/output conditions: $V_{IH}=0.8VDD$, $V_{IL}=0.2VDD$, $V_{OH}=0.8VDD$, $V_{OL}=0.2VDD$

- Any SCLK/SCLK state is allowed in the hatched area.

- **RS5C317A**

- **RS5C317B**
### FUNCTIONAL DESCRIPTIONS

#### 1. Addressing

<table>
<thead>
<tr>
<th>Address</th>
<th>Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>A3 A2 A1 A0</td>
<td>1-second counter (BANK=0)</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>S8 S4 S2 S1</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>— — — —</td>
</tr>
<tr>
<td>2 0 0 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>3 0 1 0</td>
<td>— — — —</td>
</tr>
<tr>
<td>4 0 1 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>5 1 0 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>6 1 1 0</td>
<td>— — — —</td>
</tr>
<tr>
<td>7 1 1 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>8 1 0 0</td>
<td>— — — —</td>
</tr>
<tr>
<td>9 1 0 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>A 1 0 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>B 1 0 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>C 1 1 0</td>
<td>— — — —</td>
</tr>
<tr>
<td>D 1 1 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>E 1 1 1</td>
<td>— — — —</td>
</tr>
<tr>
<td>F 1 1 1</td>
<td>— — — —</td>
</tr>
</tbody>
</table>

*1) All the listed data can be read and written.

*2) The "—" mark indicates data which can be read only and set to "0" when read.

*3) The ADJ/BSY bit of the control register is set to ADJ for write operation and BSY for read operation.

*4) The WTEN/XSTP bit of the control register is set to WTEN for write operation and XSTP for read operation.

*5) The clock/calendar counter and the alarm register can be selected when the BANK=0 and BANK=1 respectively. To designate the BANK is unnec-essary for Interrupt cycle register and Control register 1/2.

*6) The WTEN bit and TEST bit are set to "1" when CE is "Low".

*7) When the crystal oscillator is stopped after initial power-on or supply voltage drop, XSTP=1, the timer register and CLEN bit of the 32kHz control register perform as follows:

<table>
<thead>
<tr>
<th>CLEN=0</th>
<th>TM3=TM2=TM1=TMCL=0 (Timer halts)</th>
</tr>
</thead>
</table>

*8) The CLEN data can be read only and set to 0 when CLKC is "L".
2. Registers

2.1 Control Register 1 (at Eh)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTFG</td>
<td>ALFG</td>
<td>WTEN</td>
<td>ADJ</td>
</tr>
</tbody>
</table>

(For write operation)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTFG</td>
<td>ALFG</td>
<td>XSTP</td>
<td>BSY</td>
</tr>
</tbody>
</table>

(For read operation)

±30-second Adjustment Bit

<table>
<thead>
<tr>
<th>ADJ</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Ordinary operation</td>
</tr>
<tr>
<td>1</td>
<td>Second digit adjustment</td>
</tr>
</tbody>
</table>

Clock/Counter Busy-state Indication Bit

<table>
<thead>
<tr>
<th>BSY</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Ordinary operation</td>
</tr>
<tr>
<td>1</td>
<td>Second digit carry or adjustment</td>
</tr>
</tbody>
</table>

Clock Counter Enable/Disable Setting Bit

<table>
<thead>
<tr>
<th>WTEN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Disabling of 1-second digit carry for clock counter</td>
</tr>
<tr>
<td>1</td>
<td>Enabling of 1-second digit carry for clock counter</td>
</tr>
</tbody>
</table>

Oscillator Halt Sensing Bit

<table>
<thead>
<tr>
<th>XSTP</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Ordinary oscillation</td>
</tr>
<tr>
<td>1</td>
<td>Oscillator halt sensing</td>
</tr>
</tbody>
</table>

Alarm Flag Bit

<table>
<thead>
<tr>
<th>ALFG</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Unmatched alarm register with clock counter</td>
</tr>
<tr>
<td>1</td>
<td>Matched alarm register with clock counter</td>
</tr>
</tbody>
</table>

Interrupt Flag Bit

<table>
<thead>
<tr>
<th>CTFG</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>INTR-OFF enabling of write operation when CT3 bit is set to 1</td>
</tr>
<tr>
<td>1</td>
<td>INTR-L enabling of write operation when CT3 bit is set to 1</td>
</tr>
</tbody>
</table>

2.1-1 (ADJ)

The following operations are performed by setting the ADJ bit to 1.

After this bit is set to 1, the BSY bit is set to 1 for the maximum duration of 122.1µs.
If the WTEN bit is 0, these adjustment operations are started after the WTEN bit is set to 1.
1) For second digits ranging from “00” to “29” seconds:
   Time counters smaller than seconds are reset and second digits are set to “00”.
2) For second digits ranging from “30” to “59” seconds:
   Time counters smaller than seconds are reset and second digits are set to “00”. Minute digits are incremented by 1.
2.1-2 (BSY)

When the BSY bit is 1, the clock and calendar counter are being updated. Consequently, write operation should be performed for the counters when the BSY bit is 0. Meanwhile, read operation is normally performed for the counters when the BSY bit is 0, but can be performed without checking the BSY bit as long as appropriate software is provided for preventing read errors. (Refer to 15. Typical Software-based Operations.) The BSY bit is set to 1 in the following three cases:

(i) Adjustment of second digits by ±30 seconds

(ii) Second digits increment by 1 (Subject to 1-sec digit carry when the WTEN bit is switched from 0 to 1)

(iii) Ordinary 1-sec digit carry

2.1-3 (WTEN)

The WTEN bit should be set to 0 to check that the BSY bit is 0 when performing read and write operations for the clock and calendar counters. For read operation, the WTEN bit may be left as 1 without checking the BSY bit as long as appropriate measures such as read repetition are provided for preventing read errors. The WTEN bit should be set to 1 after completing read and write operations, or will automatically be set to 1 by switching the CE pin to the low level. If 1-second digit carry occurs when the WTEN bit is 0, a second digit increment by 1 occurs when the WTEN bit is set to 1. There may be a possibility causing a time delay when it takes 1/1024 second or more to set WTEN bit from 0 to 1, Read data in state of WTEN=1 in such a case. (Refer to the item 15.3)

2.1-4 (XSTP)

The XSTP bit senses the oscillator halt. When the CE pin is held at the low level, the XSTP bit is set to 1 once the crystal oscillator is stopped after initial power-on or supply voltage drop and left to be 1 after it is restarted. When the CE pin is held at the high level, the XSTP bit is left as it was when the CE pin was held at the low level without checking oscillation stop. As such, the XSTP bit can be used to validate clock and calendar count data after power-on or supply voltage drop. The XSTP bit is set to 0 when any data is written to the control register 1 (at Eh) with ordinary oscillation.

2.1-5 (ALFG)

The ALFG bit can be set to 1 when the ALE bit set to 1 with alarm interruption (INTR=L).
2.1-6 (CTFG)

The CTFG bit is set to 1 when interrupt pulses are output from the INTR pin held at the low level. There are two interrupt modes selectable: the pulse mode (when the CT3 bit is set to 0) and the level mode (when the CT3 bit is set to 1). The CTFG bit can be set only when the CT3 is set to 1. Setting the CTFG bit to 1 switches the INTR pin to the low level while setting the CTFG bit to 0 turns off the INTR pin.

<table>
<thead>
<tr>
<th>Interrupt cycle register</th>
<th>INTR output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT3 CT2 CT1 CT0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 * *1 0 0</td>
<td>OFF</td>
<td>Interrupt halt</td>
</tr>
<tr>
<td>0 * 0 1</td>
<td>ON</td>
<td>Fixing the INTR pin at low level</td>
</tr>
<tr>
<td>0 * 1 0</td>
<td>0.977ms</td>
<td>Cycle: 0.977ms (1/1024Hz) Duty 50% *2</td>
</tr>
<tr>
<td>0 * 1 1</td>
<td>0.5s</td>
<td>Cycle: 0.5s (1/2Hz) *3</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>1s</td>
<td>Every second *4</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>1 minute</td>
<td>Every minute (00 second) *4</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>10 minutes</td>
<td>Every 10 minutes (00 second) *4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(For display of second digits: 00, 10, 30, 40 and 50)</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>1 hour</td>
<td>Every hour (00 minute and 00 second) *4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(For display of minute digits: 00, 10, 20, 30, 40 and 50)</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>1 day</td>
<td>Every day (00 hour, 00 minute and 00 second a.m.) *4</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>1 week</td>
<td>Every week *4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(0 week, 0 hour, 00 minute and 00 second a.m.)</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>1 month</td>
<td>Every month *4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1 day, 0 hour, 00 minute and 00 second a.m.)</td>
</tr>
</tbody>
</table>

*1) The symbol "*" in the above table indicates 0 or 1.
*2) Cycle: 0.977ms (1/1024Hz) Duty 50%
*3) Cycle: 0.5s (1/2Hz)
*4) Every minute (00 second), 10 minutes (00 second), 1 hour (00 minute and 00 second), 1 day (0 hour, 00 minute and 00 second a.m.), 1 week (0 week, 0 hour, 00 minute and 00 second a.m.), 1 month (1 day, 0 hour, 00 minute and 00 second a.m.).
2.2 Control Register 2 (at Fh)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>12/24</td>
<td>TMR</td>
<td>BANK</td>
<td>TEST</td>
</tr>
<tr>
<td>12/24</td>
<td>TMR</td>
<td>BANK</td>
<td>TEST</td>
</tr>
</tbody>
</table>

(For write operation)
(For read operation)

Bit for Testing *1

<table>
<thead>
<tr>
<th>TEST</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Testing mode</td>
</tr>
<tr>
<td>1</td>
<td>Ordinary operation mode</td>
</tr>
</tbody>
</table>

Bank Selection Bit *2

<table>
<thead>
<tr>
<th>BANK</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Clock/calendar counter</td>
</tr>
<tr>
<td>1</td>
<td>Alarm register</td>
</tr>
</tbody>
</table>

Reset Bit for Timer Counter *3

<table>
<thead>
<tr>
<th>TMR</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Continuous timer operation</td>
</tr>
<tr>
<td>1</td>
<td>Resume timer operation after reset</td>
</tr>
</tbody>
</table>

12/24-hour Time Display System Selection Bit *4

<table>
<thead>
<tr>
<th>12/24</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>12-hour time display system (separate for mornings and afternoons)</td>
</tr>
<tr>
<td>1</td>
<td>24-hour time display system</td>
</tr>
</tbody>
</table>

*1) (TEST) Set the TEST bit to 1 in ordinary operation. TEST bit is set automatically to 1 when the CE pin is “L”.

*2) (BANK) There is no need to designate BANK bit for Interrupt cycle register and Control register 1/2.

*3) (TMR) The period for timer output is set in the “Timer register”.

*4) (12/24) The 12/24 bit specifies time digit display in BCD code.

 Either the 12-hour or 24-hour time display system should be selected before time setting.
2.3 Interrupt cycle Register (at 7h)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Bits for selecting the interrupt cycle and output mode at the INTR pin *1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT3</td>
<td>CT2</td>
<td>CT1</td>
<td>CT0</td>
<td>(For write operation)</td>
</tr>
<tr>
<td>CT3</td>
<td>CT2</td>
<td>CT1</td>
<td>CT0</td>
<td>(For read operation)</td>
</tr>
</tbody>
</table>

*1) (CT3 to CT0)
The CT3 to CT0 bits are used to select the interrupt cycle and output mode at the INTR pin. There are two interrupt modes selectable: the pulse mode (when the CT3 bit is set to 0) and the level mode (when the CT3 bit is set to 1). The interrupt cycle and output mode at the INTR pin are shown in detail in the section on the CTFG bit in “2.1 Control Register 1 (at Eh)”.

2.4 Alarm registers for day-of-the-week, 1-minute, 10-minute, 1-hour, 10-hour (BANK1, at 0h-5h)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>(For read/write) day-of-the-week 1 (at 0h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AW3</td>
<td>AW2</td>
<td>AW1</td>
<td>AW0</td>
<td>(For read/write) day-of-the-week 2 (at 1h)</td>
</tr>
<tr>
<td>ALC</td>
<td>AW6</td>
<td>AW5</td>
<td>AW4</td>
<td>(For read/write) 1-minute time digit (at 2h)</td>
</tr>
<tr>
<td>AM8</td>
<td>AM4</td>
<td>AM2</td>
<td>AM1</td>
<td>(For read/write) 10-minute time digit (at 3h)</td>
</tr>
<tr>
<td>*</td>
<td>AM40</td>
<td>AM20</td>
<td>AM10</td>
<td>(For read/write) 1-hour time digit (at 4h)</td>
</tr>
<tr>
<td>AH8</td>
<td>AH4</td>
<td>AH2</td>
<td>AH1</td>
<td>(For read/write) 10-hour time digit (at 5h)</td>
</tr>
<tr>
<td>ALE</td>
<td>*</td>
<td>AP/A, AH20</td>
<td>AH10</td>
<td></td>
</tr>
</tbody>
</table>

*1) The “*” mark in the above table indicates data which are set to 0 for read cycle and not set for write cycle.
*2) 10-hour time digit indicates AP/A and AH20 with 12-hour and 24-hour time system respectively.
*3) Make sure set an actual time-data to the alarm registers when the alarm function is activated as any imaginary alarm-data will never be match with the actual time.
*4) The INTR pin can output matched alarm interruption when the ALC bit is set 0 and halt output when the ALC bit is set to 1.
*5) The alarm function is disabled when the ALE bit is set 0 and is enables when the ALE bit is set 1.
*6) Examples of setting alarm time

<table>
<thead>
<tr>
<th>Setting alarm time</th>
<th>Day-of-the-week</th>
<th>12-hour system</th>
<th>12-hour system</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Sun.</td>
<td>Mon.</td>
<td>Tue.</td>
</tr>
<tr>
<td>AM 00:00 every day</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>AM 01:30 every day</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>AM 11: 59 every day</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PM 00:00</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>on Monday through Friday</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PM 01:30 on Sunday</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>PM 11:59 on Monday, Wednesday, and Friday</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

*7) Hour digits show “12” and “32” when the time is AM 00:00 and PM 00:00 respectively in the 12-hour system.
*8) No alarm interruption is output when all the bit from AW0 through AW6 is set to 0.
*9) Each of the AW0 through AW6 corresponds to the day-of-the-week counter such as (W4, W5, W6)=(0, 0, 0) through (1, 1, 0). Designation of day-of-the-week and AW6 through AW0 in the above table is one example.
2.5 Timer register (BANK 1, at 9h)

<table>
<thead>
<tr>
<th>TM3</th>
<th>TM2</th>
<th>TM1</th>
<th>TMCL</th>
<th>T1 (cycle time for watch-dog-timer) *3</th>
<th>T2 (time between setting TMR=1 and TMOUT output) *4</th>
<th>T3 (cycle time for free-run timer) *5</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Timer halts</td>
<td>Timer halts</td>
<td>Timer halts</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.953ms</td>
<td>1.953 to 3.907ms</td>
<td>3.906ms</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5.859ms</td>
<td>5.859 to 7.813ms</td>
<td>7.812ms</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>9.765ms</td>
<td>9.765 to 11.72ms</td>
<td>11.719ms</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>13.67ms</td>
<td>13.67 to 15.63ms</td>
<td>15.625ms</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>17.57ms</td>
<td>17.57 to 19.54ms</td>
<td>19.531ms</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>21.48ms</td>
<td>21.48 to 23.44ms</td>
<td>23.437ms</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>25.39ms</td>
<td>25.39 to 27.35ms</td>
<td>27.344ms</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>62.5ms</td>
<td>62.5 to 125ms</td>
<td>125ms</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>187.5ms</td>
<td>187.5 to 250ms</td>
<td>250ms</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>312.5ms</td>
<td>312.5 to 375ms</td>
<td>375ms</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>437.5ms</td>
<td>437.5 to 500ms</td>
<td>500ms</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>562.5ms</td>
<td>562.5 to 625ms</td>
<td>625ms</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>687.5ms</td>
<td>687.5 to 750ms</td>
<td>750ms</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>812.5ms</td>
<td>812.5 to 875ms</td>
<td>875ms</td>
</tr>
</tbody>
</table>

*1) (TMCL)
“512Hz” and “16Hz” are selectively available. When the “XSTP” bit is set to 1, the “TMCL” bit is automatically set to 0. There may be possibility to be ahead or behind of the clock counter at maximum of a halt of clock frequency (512Hz or 16Hz), when the “ADJ” bit is set to 1 in the control register-1.

*2) (TM3-TM1)
When the “XSTP” bit is set to 1 the “TM3”, “TM2”, and “TM1” is automatically set to 0, the timer counter halts.

*3) T1: The maximum disable time for timer output, TMOUT=L, after setting the “TMR” bit to 1.

*4) T2: Time between timer output and setting the “TMR” bit to 1, or setting the timer register to any value.

*5) T3: Timer output cycle time without setting “TMR” bit to 1, cycle time for free-run-timer.
6) Timing diagram for TMOUT

7) Writing operation to the timer register makes the timer counter to start operation with resetting.

2.6 32kHz control register (BANK 1, at Ah)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>CLEN (For read/write)</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
</tr>
</tbody>
</table>

*1) The "*" mark indicates data which are set to 0 for read cycle and not set for write cycle.
*2) (CLEN) control bit for 32kHz output
   The CLEN bit is set to 0 when the XSTP=1. CLEN is not writable and set to 0 when CLKC pin level low/open.

<table>
<thead>
<tr>
<th>CLKC pin</th>
<th>CLEN bit</th>
<th>32KOUT output</th>
</tr>
</thead>
<tbody>
<tr>
<td>L (open)</td>
<td>0 (prohibited to write)</td>
<td>High impedance</td>
</tr>
<tr>
<td>H</td>
<td>0</td>
<td>32kHz clock output</td>
</tr>
<tr>
<td>H</td>
<td>1</td>
<td>High impedance</td>
</tr>
</tbody>
</table>

3. Counters

3.1 Clock counter (BANK 0, at 0h-5h)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>(For read/write)</th>
<th>(at 0h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S8</td>
<td>S4</td>
<td>S2</td>
<td>S1</td>
<td>1-second time digit</td>
<td>(at 0h)</td>
</tr>
<tr>
<td>*</td>
<td>S0</td>
<td>S0</td>
<td>S0</td>
<td>10-second time digit</td>
<td>(at 1h)</td>
</tr>
<tr>
<td>M8</td>
<td>M4</td>
<td>M2</td>
<td>M1</td>
<td>1-minute time digit</td>
<td>(at 2h)</td>
</tr>
<tr>
<td>*</td>
<td>M40</td>
<td>M20</td>
<td>M10</td>
<td>10-minute time digit</td>
<td>(at 3h)</td>
</tr>
<tr>
<td>H8</td>
<td>H4</td>
<td>H2</td>
<td>H1</td>
<td>1-hour time digit</td>
<td>(at 4h)</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>P/A or H20</td>
<td>H10</td>
<td>10-hour time digit</td>
<td>(at 5h)</td>
</tr>
</tbody>
</table>

*1) The "*" mark indicates data which are set to 0 for read cycle and not set for write cycle.
*2) Any carry to 1-second digits from the second counter is disabled when the WTEN bit (of the control register 1) is set to 0.
*3) Time digit display (BCD code):
   - Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
   - Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
   - Hour digits: Range as shown in the section on the 12/24 bit and carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.
*4) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.
3.2 Day-of-the-week counter (BANK 0, at 6h)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>W4</td>
<td>W2</td>
<td>W1</td>
</tr>
</tbody>
</table>

(For read/write) Day-of-the-week counter

*1) The "*" mark indicates data which are set to 0 for read cycle and not set for write cycle.
*2) Day-of-the-week digits are incremented by 1 when carried to 1-day digits.
*3) Day-of-the-week digits display (incremented in septimal notation):
   
   \[(W4, W2, W1)= (000) \rightarrow (001) \rightarrow \cdots \rightarrow (110) \rightarrow (000)\]
   
   The relation between days of the week and day-of-the-week digits is user changeable (e.g. Sunday=000).
*4) The \((W4, W2, W1)\) should not be set to \((111)\).

3.3 Calendar counter (BANK 0, at 8h-Dh)

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8</td>
<td>D4</td>
<td>D2</td>
<td>D1</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>D20</td>
<td>D10</td>
</tr>
<tr>
<td>MO8</td>
<td>MO4</td>
<td>MO2</td>
<td>MO1</td>
</tr>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
<td>MO10</td>
</tr>
<tr>
<td>Y8</td>
<td>Y4</td>
<td>Y2</td>
<td>Y1</td>
</tr>
<tr>
<td>Y80</td>
<td>Y40</td>
<td>Y20</td>
<td>Y10</td>
</tr>
</tbody>
</table>

(For read/write) 1-day calendar digit \((at8h)\)
(For read/write) 10-day calendar digit \((at9h)\)
(For read/write) 1-month calendar digit \((atAh)\)
(For read/write) 10-month calendar digit \((atBh)\)
(For read/write) 1-year calendar digit \((atCh)\)
(For read/write) 10-year calendar digit \((atDh)\)

*1) The "*" mark indicates data which are set to 0 for read cycle and not set for write cycle.
*2) The automatic calendar function provides the following calendar digit displays in BCD code.

Day digits:
- Range from 1 to 31 (for January, March, May, July, August, October, and December).
- Range from 1 to 30 (for April, June, September, and November).
- Range from 1 to 28 (for February in ordinary years).
- Range from 1 to 29 (for February in leap years).

Carried to month digits when cycled to 1.

Month digits:
- Range from 1 to 12 and carried to year digits when cycled to 1.

Year digits:
- Range from 00 to 99 and counted as 00, 04, 08, ..., 92, and 96 in leap years.

*3) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.
USAGES

1. Read Data (For the RS5C317A)

The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the SCLK pin. The input data are registered in synchronization with the falling edge of the SCLK. When the data is read, the read cycle shall be set by control bits then registered data can be read out from SIO pin in synchronization with the rising edge of the SCLK.

**Control bits**
- **R/W**: Establishes the read mode when set to 1, and the write mode when set to 0.
- **AD**: Writes succeeding addressing bits (A3-A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
- **DT**: Writes data bits to counter or register specified by the address register set just before when set to 1 with the R/W and AD bits set equally to 0 and performs no such write operation in any other case.

**Address bits**
- **A3-A0**: Inputs the bits MSB to LSB in the address table describing the functions.

### 1.1 Read Cycle Flow

1. The CE pin is switched from “L” to “H”.
2. Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits R/W and AD are set equally to 1 while a control bit DT is set to 0. (see the SCLK 1A-8A)
3. The SIO pin enters the output mode at the rising edge of the shift clock pulse 2B from the SCLK pin while the four read bits (MSB \(\rightarrow\) LSB) at designated addresses are output at the rising edge of the shift clock pulse 5B. (see the figure below)
4. Then, the SIO pin returns to the input mode at the rising edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
5. At the end of read cycle, the CE pin is switched from “H” to “L” (after \(t_{CEH}\) from the falling edge of the eighth shift clock pulse from the SCLK pin). Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at “H”.

---

*) In the above figure, the “*” mark indicates arbitrary data; the “—” mark indicates unknown data. The “\(\bigcirc\)” mark indicates data which are available when the SIO pin is held at “H”, “L”, or Hi-z level. The diagonally shaded area of the CE and the SCLK pins indicate “H” or “L”. 

---

---

---
2. Write Data (For the RS5C317A)

Writing data to the real-time clock requires inputting setting data (control bits, address bits and data bits) to the SIO pin and then establishing the write mode by using a control bit R/W in the same manner as in read operation.

* Control bits and address bits are described in the previous section on read cycle.

- **Data bits**
  - D3-D0: Inputs the data bits MSB to LSB in the addressing table describing the functions.

2.1 Write Cycle Flow

1. The CE pin is switched from “L” to “H”.
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits R/W and DT are set equally to 0 while a control bit AD is set to 1. (see the SCLK 1A-8A)
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits R/W and AD are set equally to 0 while a control bit DT is set to 1. (see the clock 1B-8B)
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits R/W, AD, and DT are set equally to 0 (at the falling edge of shift clock pulse 5A and later from the SCLK pin) or the CE pin is switched from “H” to “L” (after tCEH from the falling edge of the eighth shift clock pulse from the SCLK pin). Following on write cycle, read operation can be performed by setting control bits in the read mode at the shift clock pulse 1C and later with the CE pin held at “H”.

*) In the above figure, the “*” mark indicates arbitrary data; and the diagonally shaded area of CE and SCLK indicates “H” or “L”.
3. Read Data (For the RS5C317B)

The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the SCLK pin. The input data are registered in synchronization with the rising edge of the SCLK. When the data is read, the read cycle shall be set by control bits then registered data can be read out from SIO pin in synchronization with the falling edge of the SCLK.

• Control bits
  - **R/W**: Establishes the read mode when set to 1, and the write mode when set to 0.
  - **AD**: Writes succeeding addressing bits (A3-A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
  - **DT**: Writes data bits to counter or register specified by the address register set just before when set to 1 with the R/W and AD bits set equally to 0 and performs no such write operation in any other case.

• Address bits
  - **A3-A0**: Inputs the bits MSB to LSB in the address table describing the functions.

3.1 Read Cycle Flow

1. The CE pin is switched from “L” to “H”.
2. Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits R/W and AD are set equally to 1 while a control bit DT is set to 0. (see the SCLK 1A-8A)
3. The SIO pin enters the output mode at the falling edge of the shift clock pulse 2B from the SCLK pin while the four read bits (MSB → LSB) at designated addresses are output at the falling edge of the shift clock pulse 5B. (see the figure below)
4. Then, the SIO pin returns to the input mode at the falling edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
5. At the end of read cycle, the CE pin is switched from “H” to “L” (after tCEH from the rising edge of the eighth shift clock pulse from the SCLK pin). Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at “H”.

*) In the above figure, the “*” mark indicates arbitrary data; the “-” mark indicates unknown data.
The “⊙” mark indicates data which are available when the SIO pin is held at “H”, “L”, or Hi-z level.
The diagonally shaded area of the CE and the SCLK pins indicate “H” or “L”.
4. Write Data (For the RS5C317B)

Writing data to the real-time clock requires inputting setting data (control bits, address bits and data bits) to the SIO pin and then establishing the write mode by using a control bit R/W in the same manner as in read operation.

* Control bits and address bits are described in the previous section on read cycle.

Data bits  D3-D0: Inputs the data bits MSB to LSB in the addressing table describing the functions

4.1 Write Cycle Flow
1. The CE pin is switched from “L” to “H”.
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits R/W and DT are set equally to 0 while a control bit AD is set to 1. (see the SCLK 1A-8A)
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits R/W and AD are set equally to 0 while a control bit DT is set to 1. (see the SCLK 1B-8B)
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits R/W, AD, and DT are set equally to 0 (at the rising edge of shift clock pulse 5A and later from the SCLK pin) or the CE pin is switched from “H” to “L” (after tCEH from the rising edge of the eighth shift clock pulse from the SCLK pin). Following on write cycle, read operation can be performed by setting control bits in the read mode at the shift clock pulse 1C and later with the CE pin held at “H”.

*) In the above figure, the “*” mark indicates arbitrary data; and the diagonally shaded area of CE and SCLK indicates “H” or “L”.

(!) Control bits and address bits are described in the previous section on read cycle.
5. CE Pin

1) Switching the CE pin to the high level enables the SCLK/SCLK and SIO pins, allowing data to be serially read from and written to the SIO pin in synchronization with shift clock pulses input from the SCLK/SCLK pin.

2) Switching the CE pin to the low level or opening disables the SCLK/SCLK and SIO pins, causing high impedance and resetting the internal interfacing circuits such as the shift register. While data of the address register and bank bit which have been written just before should be preserved.

3) The CE pin should be held at the low level or open state when no access is made to the RS5C317.

   The CE pin incorporates a pull-down resistor.

4) During system power-down (being back-up battery powered), the low-level input of the CE pin should be brought as close as possible to the VSS level to minimize the loss of charge in the battery.

5) Holding the CE pin at the high level for more than 2.5 seconds mainly forces 1Hz interrupt pulses to be output from the INTR pin for oscillation frequency measurement. When the CE pin is held at the high level for less than 1.5 seconds, no pulse is output.

6) The CE pin should be held at the low level in order to enable oscillator halt sensing. Holding the CE pin at the high level, therefore, disables oscillator halt sensing, retaining the value of the XSTP (oscillator halt sensing) bit which exists immediately before the CE pin is switched to the high level.

<table>
<thead>
<tr>
<th>Considerations</th>
</tr>
</thead>
<tbody>
<tr>
<td>When the power turns on from 0V, the CE pin should be set low or open once.</td>
</tr>
</tbody>
</table>
6. Configuration of Oscillating Circuit

![Oscillating Circuit Diagram]

Typical external device:
- X’tal : 32.768kHz
  - \( (R_I=30\,\text{k}\Omega\ \text{TYP.})\)
  - \( (C_L=6\,\text{pF}\ \text{to}\ 8\,\text{pF})\)
- \( CG=8\,\text{pF}\ \text{to}\ 20\,\text{pF} \)

Typical values of internal devices
- \( RF=15\,\text{M}\Omega\ \text{TYP.}\)
- \( RD=60\,\text{k}\Omega\ \text{TYP.}\)
- \( CD=10\,\text{pF}\ \text{TYP.}\)

*) The oscillation circuit is driven at a constant voltage of about 1.5V relative to the Vss level. Consequently, it generates a wave form having a peak-to-peak amplitude of about 1.5V on the positive side of the Vss level.

Considerations in Mounting Components Surrounding Oscillating Circuit

| 1) Mount the crystal oscillators and \( CG \) in the closest possible position to the IC. |
| 2) Avoid laying any signal or power line close to the oscillation circuit (particularly in the area marked with “← A →” in the above figure). |
| 3) Apply the highest possible insulation resistance between the OSCIN or OSCOUT pin and the PCB. |
| 4) Avoid using any long parallel line to wire the OSCIN or OSCOUT pin. |
| 5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt. |

Other Relevant Considerations

| 1) When applying an external input of clock pulses (32.768kHz) to the OSCIN pin: |
| DC coupling ............Prohibited due to mismatching input levels. |
| AC coupling...............Permissible except that unpredictable results may occur in oscillator halt sensing due to possible sensing errors caused by noises, etc. |
| 2) Avoid using the oscillator output of the RS5C317 (from the OSCOUT pin) to drive any other IC for the purpose of ensuring stable oscillation. |
7. Oscillator Halt Sensing

Oscillation Halt can be sensed through monitoring the XSTP bit with preceding setting of the XSTP bit to 0 by writing any data to the control register 1. Upon oscillator halt sensing, the XSTP bit is switched from 0 to 1. This function can be applied to judge clock data validity.

When the XSTP bit is set to 1, the timer register bits and CLEN bit perform as follows:

- CLEN = 0
- TM3 = TM2 = TM1 = TMCL = 0 (Timer halts)

\[
\begin{array}{|c|c|c|}
\hline
\text{XSTP} & \text{Power-on from 0V }^\star_1 & \text{Writing of data to control register 1} \\
& (in the presence of oscillation) & \text{Oscillation halt} \\
& & \text{Oscillation restart }^\star_2 \\
\hline
\end{array}
\]

1) While the CE pin is held at the low level, the XSTP bit is set to 1 upon power-on from 0V. Note that any instantaneous power disconnection may cause operational failure. When the CE pin is held at the high level, oscillation halt is not sensed and the value of the XSTP bit when the CE pin is held at the low level is retained.

2) Once oscillation halt has been sensed, the XSTP bit is held at 1 even if oscillation is restarted.

Considerations in Use of XSTP Bit

Ensure error-free oscillation halt sensing by preventing the following:

1) Instantaneous disconnection of VDD
2) Condensation on the crystal oscillator
3) Generation of noise on the PCB in the crystal oscillator
4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC
8. Typical Power Supply Circuit

1) Connect the capacitance of the oscillation circuit to the Vss pin.
2) Mount the high-and low-frequency by-pass capacitors in parallel and very close to the RS5C317.
3) Connect the pull-up resistor of the INTR pin to two different positions depending on whether the resistor is in use during battery back-up.
   - When not in use during battery back-up
     ..........Position A in the left figure
   - When in use during battery back-up
     ..........Position B in the left figure
4) Timing of power-on, power-off and CE pin refer to following figure.
5) When a diode are in use in place of the components surrounded by dotted lines, note that applying voltage to any input pins should be less than the rating of VDD +0.3V by using of schottky diode.

9. Oscillation Frequency Adjustment
9.1 Oscillation Frequency Measurement

1) Switch the CE pin to the high level and use a frequency counter to measure a 1Hz interrupt pulse output from the INTR pin about 2.5 seconds later.
2) Ensure that the frequency counter has more than six digits (on the order of 1 ppm).
3) Place the Cg between the OSCIN pin and the VSS level and pull up the INTR pin output to the VDD.
9.2 Oscillation Frequency Adjustment

**Select crystal oscillator**

**(For fixed capacitance)**

- Change CL value of crystal
  - Fix CG
  - Optimize CG
    - OK
      - END
    - NO

**(For variable capacitance)**

- Fix the capacitance of CG
  - Optimize central variable capacitance value
    - OK
      - END
    - NO

- Change CL value of crystal

*1) To ensure that the crystal is matched to the IC, inquire its crystal supplier about its CL (load capacitance) and R1 (equivalent series resistance) values. It is recommended that the crystal should have the CL value range of 6 to 8pF and the typical R1 value of 30kΩ.

*2) To allow for the possible effects of floating capacitance, select the optimum capacitance of the CG on the mounted PCB. The standard and recommendable capacitance values of the CG range from 5 to 24pF and 8 to 20pF, respectively. When you need to change the frequency to get higher accuracy, change the CL value of the crystal.

*3) Collate the central variable capacitance value of the CG with its oscillation frequency by adjusting the angle of rotation of the variable capacitance of the CG in such a manner that the actual variable capacitance value is slightly smaller than the central variable capacitance value. (It is recommended that the central variable capacitance value should be slightly less than one half of the actual variable capacitance value because the smaller is variable capacitance, the greater are fluctuations in oscillation frequency.) In the case of an excessive deviation of the oscillation frequency from its required value, change the CL value of the crystal.

After adjustment, oscillation frequency is subject to fluctuations of an ambient temperature and supply voltage. See “14. Typical Characteristic Measurements”.

### Note

Any rise or fall in ambient temperature from its reference value ranging from 20 to 25 degrees Celsius causes a time delay for a 32kHz crystal oscillator. It is recommendable, therefore, to set slightly high oscillation frequency at room temperature.
10. Interrupt Operation

Two interrupt operations are available:

1) Alarm interrupt........When a registered time for alarm (such as day-of-the-week, hour or minute) coincide with calendar counter (such as day-of-the-week, hour or minute) interrupt to the CPU are requested with INTR pin or ALRM pin being “L” (ON).

2) Periodic interrupt ......The INTR pin comes to a “L” (ON) state every registered period outputting interrupt request.

Function diagram of alarm and periodic interrupts are shown as follows:

---

10.1 Alarm Interrupt

For setting an alarm time, designated time such as day-of-the-week, hour or minute should be set to the alarm registers being ALE bit to 0. After that set the ALE bit to 1, from this moment onward when such registered alarm time coincide with the value of calendar counter the ALRM comes down to Low (ON). The ALRM output can be controlled by operating to the ALE and ALFG bits.

---

*1) Setting the ALC into 1 halt output of the alarm interrupt from INTR pin.

*2) Both of alarm and periodic interrupt can operate regardless of the state of CE pin, “H” or “L”.

---

*1) The * "mark indicates the time when the registered alarm day-of-the-week and time coincide with calendar counter.

*2) Above figure describes in case of no periodic interruption.

*3) ALFG indicates a reverse state of ALRM output.
10.2 Periodic (Clock) Interrupt

The INTR pin output, the interrupt cycle register, and the CTFG bit can be used to interrupt the CPU in a certain cycle. The interrupt cycle register can be used to select either one of two interrupt output modes: the pulse mode (when the CT3 bit is set to 0) and the level mode (when the CT3 bit is set to 1).

10.2-1 Interrupt Cycle Selection

<table>
<thead>
<tr>
<th>Interrupt cycle register</th>
<th>INTR output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT3 CT2 CT1 CT0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>OFF</td>
<td>Interrupt halt</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>ON</td>
<td>Fixing the INTR pin to the low level</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>0.977ms</td>
<td>Cycle: 0.977ms (1/1024Hz) Duty 50%</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>0.5s</td>
<td>Cycle: 0.5s (1/2Hz)</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>1s</td>
<td>Every second</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>10s</td>
<td>Every 10 seconds (For display of second digits: 00, 10, 20, 30, 40 and 50)</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>1 min</td>
<td>Every minute (00 second)</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>10 min</td>
<td>Every 10 minutes (For display of minute digits: 00, 10, 20, 30, 40 and 50)</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>1 hour</td>
<td>Every hour (00 minute and 00 second)</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>1 day</td>
<td>Every day (0 hour, 00 minute and 00 second a.m.)</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>1 week</td>
<td>Every week (0 week, 0 hour, 00 minute and 00 second a.m.)</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>1 month</td>
<td>Every month (1st day, 0 hour, 00 minute and 00 second a.m.)</td>
</tr>
</tbody>
</table>

*1) The "*" mark indicates 0 or 1.

10.2-2 Pulse mode Interrupt

When the CT3 bit is set to 0 and provides four interrupt cycles, off, on, 1024Hz, and 2Hz can be selected. The CTFG bit cannot be set because it is used for output monitoring.

\[
\begin{align*}
\text{CTFG} & \quad \text{INTR} \\
\text{T1} & \quad \text{0.488ms} \\
\end{align*}
\]

1024Hz : T1= 0.977ms

2Hz : T1= 500ms

10.2-3 Level mode Interrupt

When the CT3 bit is set to 1, clock-interlocked cycles in increments of one second to one month can be selected. The CTFG bit can be written; writing 1 to the CTFG bit switches the INTR pin to the low level while writing 0 to the CTFG bit turns off the INTR pin.

\[
\begin{align*}
\text{CTFG} & \quad \text{INTR} \\
\end{align*}
\]

Interrupt (Second count-up) Interrupt (Second count-up)

Writing 0 to CTFG bit
11. Timer

TMOUT outputs periodic pulses every registered time period (in BANK=1, at 9h). Setting TMR bit to 1 makes the timer counter reset and possible to operate as a watch-dog-timer.

- **TMOUT**
- **MAX. T1**
- **T2**
- **T3**
- **TMR<–1**
- **TMR<–1**
- **0.977 ms**

*1) Timer counter is available when the CE pin is set 0.
*2) Timer function is disabled when the XSTP bit is set to 1.
   (TM3 to TM1 and TMCL of timer register become to 0)
*3) Refer to “Timer register” in FUNCTION section regarding to T1, T2, and T3 in the above figure.
*4) TMOUT will be OFF when the TMR bit is set to one with TMOUT=L (ON)
*5) Write operation to the timer registers causes starting to operate of timer counter after resetting.

12. 32kHz Clock Output

Clock signal of 32kHz crystal oscillator can be output from the 32KOUT pin. When this function is disabled the 32KOUT pin is held at high impedance.

32kHz clock output can be controlled through CLKC pin and CLEN pin.

<table>
<thead>
<tr>
<th>CLKC pin</th>
<th>CLEN bit</th>
<th>32KOUT output</th>
</tr>
</thead>
<tbody>
<tr>
<td>L (open)</td>
<td>0 (disabled to write)</td>
<td>High impedance</td>
</tr>
<tr>
<td>H</td>
<td>0</td>
<td>Output 32kHz clock</td>
</tr>
<tr>
<td>H</td>
<td>1</td>
<td>High impedance</td>
</tr>
</tbody>
</table>

*1) CLKC pin incorporates pulled down resistor.
*2) The CLEN bit will be set to 0 when the XSTP bit is set to 1.
   The conditions of the XSTP bit being set to 1 is as follows:
   (I) Initial power-on    (II) Supply voltage drop  (III) Crystal oscillation halt
*3) Do not hold the CLKC pin at high level when initial power on.
13. Typical Application

*1) Connect the capacitance of the oscillation circuit to the VSS pin.
*2) Mount the high-and low-frequency by-pass capacitors in parallel and very close to the RS5C317.
*3) Connect the pull-up resistor of the INTR pin or ALRM pin to two different positions depending on whether the resistor is in use during battery back-up:
   (I) When not in use during battery back-up...........Position A in the above figure
   (II) When in use during battery back-up...............Position B in the above figure
*4) When using a “D” circuit in place of “C”, note that forward voltage of diode should be minimized to eliminate applying excess voltage to input pins.
   (Take the utmost care on system powering-ON and-OFF).
14. Typical Characteristic Measurements

14.1 Standby Current vs. Cg

\[
\begin{align*}
\text{Standby Current (\mu A)} & \quad \text{Topt} = 25^\circ C \\
0 & \quad 0.0 \\
1.0 & \quad 1.0 \\
2.0 & \quad 2.0 \\
\end{align*}
\]

\[
\begin{align*}
C_g (\text{pF}) & \quad V_{DD} = 5V \\
0 & \quad 0 \\
10 & \quad 1 \\
20 & \quad 2 \\
30 & \quad 3 \\
\end{align*}
\]

14.2 Standby Current vs. VDD

\[
\begin{align*}
\text{Standby Current (\mu A)} & \quad \text{Topt} = 25^\circ C \\
0.0 & \quad 0 \\
1.0 & \quad 1 \\
2.0 & \quad 2 \\
\end{align*}
\]

\[
\begin{align*}
V_{DD} (V) & \quad C_g = 10\text{pF} \\
0 & \quad 0 \\
2 & \quad 2 \\
4 & \quad 4 \\
6 & \quad 6 \\
\end{align*}
\]

14.3 Operational Current vs. SCLK/SCLK Frequency

\[
\begin{align*}
\text{Operational Current (mA)} & \quad \text{Topt} = 25^\circ C \\
0.001 & \quad 0.01 \\
0.01 & \quad 0.1 \\
0.1 & \quad 1.0 \\
1.0 & \quad 10.0 \\
\end{align*}
\]

\[
\begin{align*}
\text{SCLK/SCLK Frequency (MHz)} & \quad V_{DD} = 5V \\
0.01 & \quad 0.1 \\
0.1 & \quad 1.0 \\
1.0 & \quad 10.0 \\
\end{align*}
\]

14.4 Standby Current vs. Temperature

\[
\begin{align*}
\text{Standby Current (\mu A)} & \quad C_g = 10\text{pF} \\
0.0 & \quad 0 \\
1.0 & \quad 1 \\
2.0 & \quad 2 \\
\end{align*}
\]

\[
\begin{align*}
\text{Temperature Topt (°C)} & \quad V_{DD} = 6V \\
-60 & \quad -60 \\
-40 & \quad -40 \\
-20 & \quad -20 \\
0 & \quad 0 \\
20 & \quad 20 \\
40 & \quad 40 \\
60 & \quad 60 \\
80 & \quad 80 \\
100 & \quad 100 \\
\end{align*}
\]
14.5 Oscillation Frequency Deviation vs. $C_G$
\textit{(f0: $C_G=10\text{pF}$ reference)}

$V_{DD} = 3\text{V}, T_{opt} = 25\degree\text{C}$

14.6 Oscillation Frequency Deviation vs. $V_{DD}$
\textit{(f0: $V_{DD}=4\text{V}$ reference)}

$C_G = 10\text{pF}, T_{opt} = 25\degree\text{C}$

14.7 Oscillation Frequency Deviation vs. Temperature \textit{(f0: $T_{opt}=25\degree\text{C}$ reference)}

$V_{DD} = 3\text{V}, C_G = 10\text{pF}$

14.8 Oscillation Start Time vs. $V_{DD}$

$T_{opt} = 25\degree\text{C}$

14.9 $V_{DS}$ vs. $I_{DS}$ for Nch Open Drain Output

$T_{opt} = 25\degree\text{C}$

14.10 $I_{IH}$ vs. $V_{IH}$ for CLKC pin

$T_{opt} = 25\degree\text{C}$
15. Typical Software-based Operations

15.1 Initialization upon Power-on

Ensure stable oscillation by preventing the following:

1) Condensation on the crystal oscillator
2) Instantaneous disconnection of power
3) Generation of clock noises, etc, in the crystal oscillator
4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC

*1) Switch the CE pin to the low level immediately after power-on.

*2) When not making oscillation halt sensing (data validity), the XSTP bit need not be checked.

*3) Turn off the INTR pin, whose output is uncertain at power-on.

*4) Set the ADJ bit to 1. When writing control register 1, if the oscillator has operated, the XSTP bit is changed from 1 to 0.

*5) It takes about 0.1 to 2 seconds to be set the BSY bit to 0 from oscillation starting upon power-on from 0V. Provide an exit from an oscillation start loop to prepare for oscillation failure.

*6) Set the XSTP bit to 0 by writing data to the control register 1, and set to the control register 2.

When Using the XSTP Bit

<table>
<thead>
<tr>
<th>Ensure stable oscillation by preventing the following:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Condensation on the crystal oscillator</td>
</tr>
<tr>
<td>2) Instantaneous disconnection of power</td>
</tr>
<tr>
<td>3) Generation of clock noises, etc, in the crystal</td>
</tr>
<tr>
<td>oscillator</td>
</tr>
<tr>
<td>4) Charge of voltage exceeding prescribed maximum</td>
</tr>
<tr>
<td>ratings to the individual pins of the IC</td>
</tr>
</tbody>
</table>

15.2 Write Operation to Clock and Calendar Counters

*1) After switching the CE pin to the high level, hold it at the high level until any subsequent operation requires switching it to the low level. (Note that switching the CE pin to the low level sets the WTEN bit to 1.)

*2) WTEN bit is set to 0.

*3) The BSY bit is held at 1 for a maximum duration of 122.1µs.

*4) Switch the CE pin to the low level to set the WTEN bit to 1. During write operation to the clock and calendar counters, one 1-second digit carry causes a 1-second increment while two 1-second digit carries also cause only a 1-seconds increment, which, in turn, causes a time delay.
### 15.3 Read Operation from Clock and Calendar Counters

#### 15.3-1

- **CE=H**
- Control register $\leftarrow 0h$
- **BSY=0?**
  - NO
  - **CE=L**
  - Wait or other operations.
- **CE=L**

#### 15.3-2

- **Read 1-second digit of clock counter.**
- **Read from clock and calendar counters.**
- **CE=L**
- Again read 1-second digit of clock counter.
- **NO**
  - Two 1-second digit readings match?
  - **YES**

**Note**

Read data as described in 15.3-2 or 15.3-3 when it takes (1/1024) sec or more to set the WTEN bit from 0 to 1 (CE=L), the read operation described in 15.3-1 is prohibited as such a case.

#### 15.3-3

- **Interrupt to CPU**
  - **CTFG=1?**
  - NO
  - Control register $\leftarrow 2h$
  - Interrupt operation from any other IC
- **YES**
  - Read from clock and calendar counters.

**Notes**

1. to 4. These notes are the same as 15.2 notes 1) to 4).
2. When needing any higher-order digits than the minute digits, replace second digits with minute digits. (Reading LSD one of the required digits twice.)
3. Select the level mode as an interrupt mode by setting the CT3 bit to 1.
4. Write 0 to CTFG bit for turning off INTR pin.
5. Complete read operation within an interrupt cycle after interrupt generation. (e.g. within 1 second)
15.4 Write Operation to Alarm time

- Set alarm (hour or minute, day of the week) *1
- ALE ← 1

*1) Non-existent alarm can set in the alarm registers, but when it sets, an alarm interrupt is disabled. To enable an alarm interrupt, existent alarm time must be set in the alarm registers.

15.5 Second-digit Adjustment by ±30 seconds

- Control register 1 ← 3h *1

*1) Set the ADJ bit to 1.
(The BSY bit is held at 1 for a maximum duration of 122.1µs after the ADJ bit is set to 1.)

15.6 Oscillation Start Judgment

- Power-on

**YES**
- XSTP = 0?
  **NO**
  - Control register 1 ← 2h
  - CE ← “L”

**YES**
- Wait or other operations.

*1) The XSTP bit is set to 1 upon power-on from 0V.

*2) It takes approximately 0.1 to 2 seconds to start oscillation. Provide an exit from an oscillation start loop to prepare for oscillation failure.

When Using the XSTP Bit

Ensure stable oscillation by preventing the following:
1) Condensation on the crystal oscillator
2) Instantaneous disconnection of power
3) Generation of clock noises, etc, in the crystal oscillator
4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC
15.7 Interrupt Operation
15.7-1 Cyclic Interrupt Operation

Set interrupt cycle register

CTFG=1? [YES] Control register 1→2h [NO] Cyclic interrupt operation

Interrupt to CPU

*1) Set the interrupt cycle register to the level mode by setting the CTS bit to 1.

*2) Write 0 to CTFG bit for turning off INTR pin.

15.7-2 Alarm Interrupt Operation

Set alarm (hour or minute, day-of the week)

ALE←1

Interrupt to CPU

ALFG=1? [NO] Interrupt operation from any other IC [YES] ALFG←0

*1) Write 0 to ALFG bit for turning off ALRM pin.
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