RICOH

Microprocessor power management with Watchdog Timer

R5101G SERIES

NO. EA-071-071025

OUTLINE

The R5101G Series are CMOS-based μ con power management ICs with high accuracy output voltage and detector threshold and with ultra low supply current. Each of these ICs consists of a voltage regulator, a voltage detector and a watchdog timer. Thus, the R5101G Series have the function of a power management for microprocessor, a monitor of the voltage of a power source and a microprocessor supervisor.

The built-in voltage regulator with an internal driver transistor can supply typically 50mA current to a system when the voltage difference between input and output is 2V. Therefore these ICs are very suitable for various power supply systems for microprocessors. The output voltage is monitored by the voltage detector which is built-in these ICs.

The built-in voltage detector has an output delay function and the delay time can be set by an external capacitor (C_D).

The output voltage and the detector threshold voltage can be set individually for each IC by laser trimming.

Furthermore, when a microprocessor works incorrectly, the watchdog timer which checks over microprocessor generates reset signals intermittently to prevent a whole system from being malfunction.

The timeout periods for watchdog and reset can also be set individually by an external capacitor (C_{TW}).

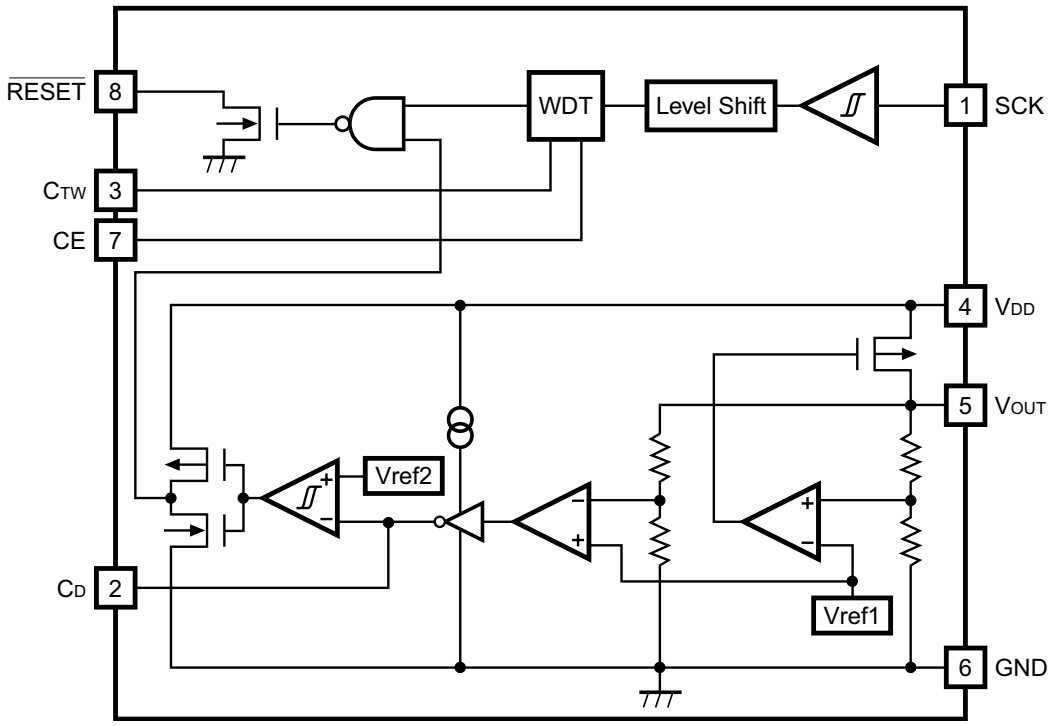
FEATURES

- Built-in a watchdog timer
- Timeout period for watchdog and generating a reset signal can be set by an external capacitor
- Watchdog timer can be stopped individually by CE Pin
- Low supply current ····· Typ. 5μA
- The output voltage of Voltage Regulator and the detector threshold voltage can be set individually with a step of 0.1V for each IC by laser-trim.
- High Accuracy Output Voltage of Voltage Regulator and Detector Threshold ····· ±2.5%
- Power-on Reset Delay Time can be set by an external capacitor
- Output Current ····· Typ. 50mA (at V_{IN} - V_{OUT}=2V)
- Small Package ····· Ultra-mini SSOP-8G (0.65mm pitch)

APPLICATION

- Power source for microprocessors

BLOCK DIAGRAMS



SELECTION GUIDE

The selection can be made with designating the part number as shown below:

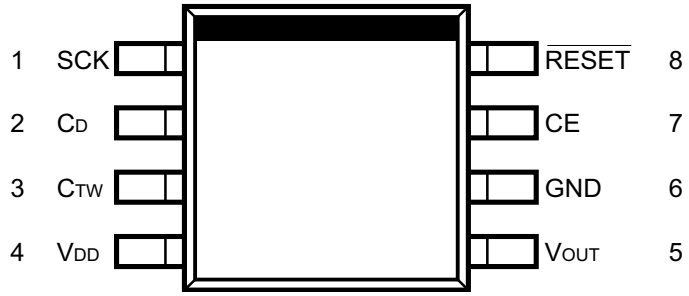
R5101Gxxxx-TR ←part Number

↑ ↑ ↑

a b c

Code	Descriptions
a	Designation of Package Type; G:SSOP8G
b	Serial Number for Voltage setting from001
c	Alphabetical Code for Mask Versions A:Standard

PIN CONFIGURATION



SSOP8G (0.65mm pitch)

PIN DESCRIPTION

Pin No	Symbol	Pin Description
1	SCK	Clock Input Pin from Microprocessor
2	C_D	External Capacitor Pin for Setting Delay Time of Voltage Detector
3	C_{TW}	External Capacitor Pin for Setting Reset and Watchdog Timeout Periods
4	V_{DD}	Power supply Pin
5	V_{OUT}	Output Pin for Voltage Regulator
6	GND	Ground Pin
7	CE	Control Switch Pin for Watchdog timer (“H” active, “L” inactive)
8	$\overline{\text{RESET}}$	Output Pin for Reset signal of Watchdog timer and Voltage Detector. (Output Type is Nch Open Drain, Output “L” at detecting Detector Threshold and Watchdog Timer Reset.)

ABSOLUTE MAXIMUM RATINGS

Topt=25°C, Vss=0V

Symbol	Item		Rating	Unit
V_{DD}	Supply Voltage		-0.3~12	V
V_{CD}	Output Voltage	Voltage of C_D Pin	V_{SS}-0.3~V_{DD}+0.3	V
V_{CTW}		Voltage of C_{TW} Pin	V_{SS}-0.3~V_{DD}+0.3	V
V_{OUT}		Voltage of V_{OUT} Pin	V_{SS}-0.3~V_{DD}+0.3	V
$V_{\overline{RESET}}$		Voltage of $\overline{\text{RESET}}$ Pin	V_{SS} -0.3~12	V
$V_{\overline{RESET}}$	Input Voltage	Voltage of CE Pin	V_{SS} -0.3~V_{DD}+0.3	V
V_{CE}		Voltage of SCK Pin	V_{SS} -0.3~V_{DD}+0.3	V
I_{OUT}	Output Current	Current of V_{OUT} Pin	150	mA
$I_{\overline{RESET}}$		Current of $\overline{\text{RESET}}$ Pin	10	mA
P_D	Power Dissipation		300	mW
Topt	Operating Temperature Range		-40~+85	°C
Tstg	Storage Temperature Range		-55~+125	°C

ELECTRICAL CHARACTERISTICS

R5101G001A Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage				10	V
Iss-On	Supply Current (WDT active)	V_{DD}=CE=5.0V		5	15	μA
Iss-Off	Supply Current (WDT inactive)	V_{DD}=5.0V, CE=GND		6	18	μA
V_{OUT}	Output Voltage	V_{DD}=5.0V, I_{OUT}=10mA	2.925	3.000	3.075	V
I_{OUT}	Output Current	V_{DD}=5.0V	50			mA
V_{DIF}	Dropout Voltage	I_{OUT}=30mA	150	500	850	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{DD}=5.0V 1mA≤I_{OUT}≤50mA		50	100	mV
$\Delta V_{OUT}/\Delta V_{DD}$	Line Regulation	I_{OUT}=10mA V_{OUT}+0.5V≤V_{DD}≤10V		0.1	0.2	%/V
I_{LIM}	Current Limit (Short mode)	V_{OUT}=GND	10	50	100	mA
ΔV_{OUT}/ ΔTopt	Output Voltage Temperature Coefficient	I_{OUT}=10mA -40°C≤Topt≤85°C		±100		ppm/ °C
$-V_{DET}$	Detector Threshold		2.633	2.700	2.767	V
V_{HYS}	Hysteresis Range		0.081	0.135	0.189	V
V_{DETMGN}	Regulator Voltage Margin against Released Voltage	V_{OUT}-((-V_{DET})+V_{HYS}), I_{OUT}=10mA	0.02			V
Δ-V_{DET}/ ΔTopt	Detector Threshold Temperature Coefficient	-40°C≤Topt≤85°C		±100		ppm/ °C
t_{PR}	Reset Delay Time	V_{DD}=5.0V, CD=0.001μF	7	14	21	ms
t_{WD}	Watchdog Timeout period	V_{DD}=5.0V, CW=0.01μF	50	100	150	ms
t_{WR}	Reset Hold Time of WDT	V_{DD}=5.0V, CW=0.01μF	5	10	15	ms
V_{IHSCK}	SCK Input Voltage “H”	V_{DD}=5.0V	0.8× V_{OUT}		V_{DD}	V
V_{ILSCK}	SCK Input Voltage “L”	V_{DD}=5.0V	0.0		0.2× V_{OUT}	V
V_{IHCE}	CE Input Voltage “H”		1.2		V_{DD}	V
V_{ILCE}	CE Input Voltage “L”		0.0		0.2	V
I_{IHSCK}	SCK Input Current “H”	V_{DD}=SCK=5.0V	-1		1	μA
I_{ILSCK}	SCK Input Current “L”	V_{DD}=5.0V, SCK=GND	-1		1	μA
R_{PU}	CE Pull-up Resistance		2	4	10	MΩ
I_{CD}	C_D Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
I_{CTW}	C_{TW} Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
$I_{\overline{RESET}}$	$\overline{RESET}$ Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
Ileak	$\overline{RESET}$ Pin Leakage Current	V_{DD}=10.0V,CE=GND, V_{DS}=10.0V	-1		1	μA
T_{SCKW}	SCK Input Pulse Width	V_{DD}=5.0V	500			ns
Vstart	Minimum Operating Voltage of Voltage Detector			0.9	1.5	V

R5101G002A

Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage				10	V
Iss-On	Supply Current (WDT active)	V_{DD}=CE=5.3V		5	15	μA
Iss-Off	Supply Current (WDT inactive)	V_{DD}=5.3V, CE=GND		6	18	μA
V_{OUT}	Output Voltage	V_{DD}=5.3V, I_{OUT}=10mA	3.218	3.300	3.382	V
I_{OUT}	Output Current	V_{DD}=5.3V	50			mA
V_{DIF}	Dropout Voltage	I_{OUT}=30mA	100	500	850	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{DD}=5.3V 1mA≤I_{OUT}≤50mA		50	100	mV
$\Delta V_{OUT}/\Delta V_{DD}$	Line Regulation	I_{OUT}=10mA V_{OUT}+0.5V≤V_{DD}≤10V		0.1	0.2	%/V
I_{LIM}	Current Limit (Short mode)	V_{OUT}=GND	10	50	100	mA
$\Delta V_{OUT}/\Delta Topt$	Output Voltage Temperature Coefficient	I_{OUT}=10mA -40°C≤Topt≤85°C		±100		ppm/°C
$-V_{DET}$	Detector Threshold		2.925	3.000	3.075	V
V_{HYS}	Hysteresis Range		0.090	0.150	0.210	V
V_{DETMGN}	Regulator Voltage Margin against Released Voltage	V_{OUT}-((-V_{DET})+V_{HYS}), I_{OUT}=10mA	0.02			V
Δ-$V_{DET}/\Delta Topt$	Detector Threshold Temperature Coefficient	-40°C≤Topt≤85°C		±100		ppm/°C
t_{PR}	Reset Delay Time	V_{DD}=5.3V, C_D=0.001μF	7	14	21	ms
t_{WD}	Watchdog Timeout period of WDT	V_{DD}=5.3V, CW=0.01μF	50	100	150	ms
t_{WR}	Reset Hold Time of WDT	V_{DD}=5.3V, CW=0.01μF	5	10	15	ms
V_{IHSCK}	SCK Input Voltage “H”	V_{DD}=5.3V	0.8× V_{OUT}		V_{DD}	V
V_{ILSCK}	SCK Input Voltage “L”	V_{DD}=5.3V	0.0		0.2× V_{OUT}	V
V_{IHCE}	CE Input Voltage “H”		1.2		V_{DD}	V
V_{ILCE}	CE Input Voltage “L”		0.0		0.2	V
I_{IHSCK}	SCK Input Current “H”	V_{DD}=SCK=5.3V	-1		1	μA
I_{ILSCK}	SCK Input Current “L”	V_{DD}=5.3V, SCK=GND	-1		1	μA
R_{PU}	CE Pull-up Resistance		2	4	10	MΩ
I_{CD}	C_D Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
I_{CTW}	C_{TW} Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
$I_{\overline{RESET}}$	$\overline{RESET}$ Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
Ileak	$\overline{RESET}$ Pin Leakage Current	V_{DD}=10.0V, CE=GND, V_{DS}=10.0V	-1		1	μA
T_{SCKW}	SCK Input Pulse Width	V_{DD}=5.3V	500			ns
Vstart	Minimum Operating Voltage of Voltage Detector			0.9	1.5	V

R5101G003A

Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage				10	V
Iss-On	Supply Current (WDT active)	V_{DD}=CE=7.0V		7	20	μA
Iss-Off	Supply Current (WDT inactive)	V_{DD}=7.0V, CE=GND		8	24	μA
V_{OUT}	Output Voltage	V_{DD}=7.0V, I_{OUT}=10mA	4.875	5.000	5.125	V
I_{OUT}	Output Current	V_{DD}=7.0V	50			mA
V_{DIF}	Dropout Voltage	I_{OUT}=30mA	100	350	650	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{DD}=7.0V 1mA≤I_{OUT}≤50mA		50	100	mV
$\Delta V_{OUT}/\Delta V_{DD}$	Line Regulation	I_{OUT}=10mA V_{OUT}+0.5V≤V_{DD}≤10V		0.1	0.2	%/V
I_{LIM}	Current Limit (Short mode)	V_{OUT}=GND	10	50	100	mA
ΔV_{OUT}/ ΔTopt	Output Voltage Temperature Coefficient	I_{OUT}=10mA -40°C≤Topt≤85°C		±100		ppm/ °C
$-V_{DET}$	Detector Threshold		4.388	4.500	4.612	V
V_{HYS}	Hysteresis Range		0.135	0.225	0.315	V
V_{DETMGS}	Regulator Voltage Margin against Released Voltage	V_{OUT}-((-V_{DET})+V_{HYS}), I_{OUT}=10mA	0.02			V
Δ-V_{DET}/ ΔTopt	Detector Threshold Temperature Coefficient	-40°C≤Topt≤85°C		±100		ppm/ °C
t_{PR}	Reset Delay Time	V_{DD}=7.0V, C_D=0.001μF	7	14	21	ms
t_{WD}	Watchdog Timeout period of WDT	V_{DD}=7.0V, CW=0.01μF	50	100	150	ms
t_{WR}	Reset Hold Time of WDT	V_{DD}=7.0V, CW=0.01μF	5	10	15	ms
V_{IHSCK}	SCK Input Voltage “H”	V_{DD}=7.0V	0.8× V_{OUT}		V_{DD}	V
V_{ILSCK}	SCK Input Voltage “L”	V_{DD}=7.0V	0.0		0.2× V_{OUT}	V
V_{IHCE}	CE Input Voltage “H”		1.2		V_{DD}	V
V_{ILCE}	CE Input Voltage “L”		0.0		0.2	V
I_{IHSCK}	SCK Input Current “H”	V_{DD}=SCK=7.0V	-1		1	μA
I_{ILSCK}	SCK Input Current “L”	V_{DD}=7.0V, SCK=GND	-1		1	μA
R_{PU}	CE Pull-up Resistance		2	4	10	MΩ
I_{CD}	C_D Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
I_{CTW}	C_{TW} Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
$I_{\overline{RESET}}$	$\overline{\text{RESET}}$ Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
Ileak	$\overline{\text{RESET}}$ Pin Leakage Current	V_{DD}=10.0V, CE=GND, V_{DS}=10.0V	-1		1	μA
T_{SCKW}	SCK Input Pulse Width	V_{DD}=7.0V	500			ns
Vstart	Minimum Operating Voltage of Voltage Detector			0.9	1.5	V

R5101G004A Topt=25°C

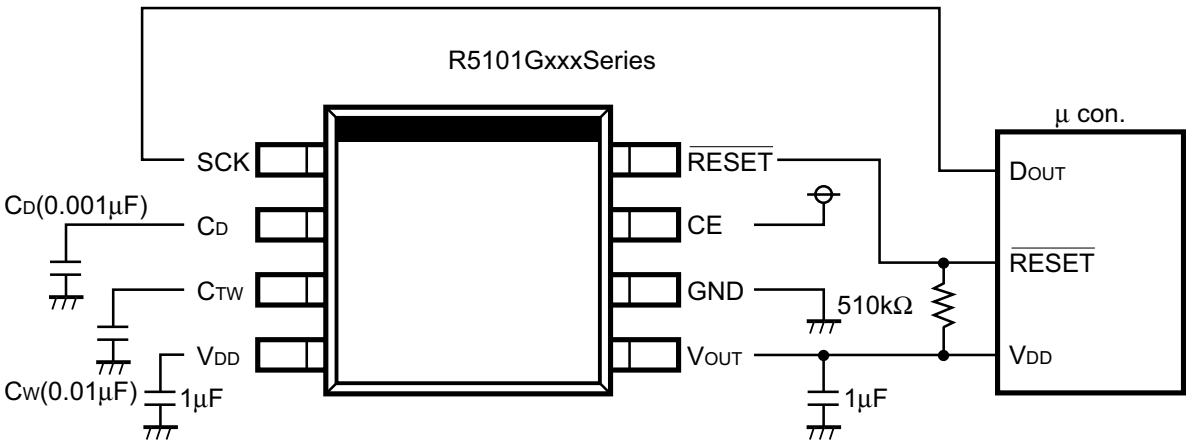
Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage				10	V
Iss-On	Supply Current (WDT active)	V_{DD}=CE=7.0V		7	20	μA
Iss-Off	Supply Current (WDT inactive)	V_{DD}=7.0V, CE=GND		8	24	μA
V_{OUT}	Output Voltage	VDD=7.0V, I_{OUT}=10mA	4.875	5.000	5.125	V
I_{OUT}	Output Current	V_{DD}=7.0V	50			mA
V_{DIF}	Dropout Voltage	I_{OUT}=30mA	100	350	650	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{DD}=7.0V 1mA≤I_{OUT}≤50mA		50	100	mV
$\Delta V_{OUT}/\Delta V_{DD}$	Line Regulation	I_{OUT}=10mA V_{OUT}+0.5V≤V_{DD}≤10V		0.1	0.2	%/V
I_{LIM}	Current Limit (Short mode)	V_{OUT}=GND	10	50	100	mA
$\Delta V_{OUT}/\Delta Topt$	Output Voltage Temperature Coefficient	I_{OUT}=10mA -40°C≤Topt≤85°C		±100		ppm/°C
$-V_{DET}$	Detector Threshold		2.145	2.200	2.255	V
V_{HYS}	Hysteresis Range		0.066	0.110	0.154	V
V_{DETMGN}	Regulator Voltage Margin against Released Voltage	V_{OUT}-((-V_{DET})+V_{HYS}), I_{OUT}=10mA	0.02			V
Δ-$V_{DET}/\Delta Topt$	Detector Threshold Temperature Coefficient	-40°C≤Topt≤85°C		±100		ppm/°C
t_{PR}	Reset Delay Time	V_{DD}=7.0V, CD=0.001μF	7	14	21	ms
t_{WD}	Watchdog Timeout period of WDT	V_{DD}=7.0V, CW=0.01μF	50	100	150	ms
t_{WR}	Reset Hold Time of WDT	V_{DD}=7.0V, CW=0.01μF	5	10	15	ms
V_{IHSCK}	SCK Input Voltage “H”	V_{DD}=7.0V	0.8× V_{OUT}		V_{DD}	V
V_{ILSCK}	SCK Input Voltage “L”	V_{DD}=7.0V	0.0		0.2× V_{OUT}	V
V_{IHCE}	CE Input Voltage “H”		1.2		V_{DD}	V
V_{ILCE}	CE Input Voltage “L”		0.0		0.2	V
I_{IHSCK}	SCK Input Current “H”	V_{DD}=SCK=7.0V	-1		1	μA
I_{ILSCK}	SCK Input Current “L”	V_{DD}=7.0V, SCK=GND	-1		1	μA
R_{PU}	CE Pull-up Resistance		2	4	10	MΩ
I_{CD}	C_D Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
I_{CTW}	C_{TW} Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
$I_{\overline{RESET}}$	$\overline{RESET}$ Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
Ileak	$\overline{RESET}$ Pin Leakage Current	V_{DD}=10.0V, CE=GND, V_{DS}=10.0V	-1		1	μA
T_{SCKW}	SCK Input Pulse Width	V_{DD}=7.0V	500			ns
Vstart	Minimum Operating Voltage of Voltage Detector			0.9	1.5	V

R5101G005A

Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage				10	V
Iss-On	Supply Current (WDT active)	V_{DD}=CE=4.8V		5	15	μA
Iss-Off	Supply Current (WDT inactive)	V_{DD}=4.8V, CE=GND		6	18	μA
V_{OUT}	Output Voltage	V_{DD}=4.8V, I_{OUT}=10mA	2.730	2.800	2.870	V
I_{OUT}	Output Current	V_{DD}=4.8V	50			mA
V_{DIF}	Dropout Voltage	I_{OUT}=10mA	100	350	650	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{DD}=4.8V 1mA≤I_{OUT}≤50mA		50	100	mV
$\Delta V_{OUT}/\Delta V_{DD}$	Line Regulation	I_{OUT}=10mA V_{OUT}+0.5V≤V_{DD}≤10V		0.1	0.2	%/V
I_{LIM}	Current Limit (Short mode)	V_{OUT}=GND	10	50	100	mA
$\Delta V_{OUT}/\Delta Topt$	Output Voltage Temperature Coefficient	I_{OUT}=10mA -40°C≤Topt≤85°C		±100		ppm/°C
$-V_{DET}$	Detector Threshold		2.340	2.400	2.460	V
V_{HYS}	Hysteresis Range		0.072	0.120	0.168	V
V_{DETMGN}	Regulator Voltage Margin against Released Voltage	V_{OUT}-((-V_{DET})+V_{HYS}), I_{OUT}=10mA	0.02			V
$\Delta -V_{DET}/\Delta Topt$	Detector Threshold Temperature Coefficient	-40°C≤Topt≤85°C		±100		ppm/°C
t_{PR}	Reset Delay Time	V_{DD}=4.8V, CD=0.001μF	7	14	21	ms
t_{WD}	Watchdog Timeout period of WDT	V_{DD}=4.8V, CW=0.01μF	50	100	150	ms
t_{WR}	Reset Hold Time of WDT	V_{DD}=4.8V, CW=0.01μF	5	10	15	ms
V_{IHSCK}	SCK Input Voltage “H”	V_{DD}=4.8V	0.8× V_{OUT}		V_{DD}	V
V_{ILSCK}	SCK Input Voltage “L”	V_{DD}=4.8V	0.0		0.1× V_{OUT}	V
V_{IHCE}	CE Input Voltage “H”		1.2		V_{DD}	V
V_{ILCE}	CE Input Voltage “L”		0.0		0.2	V
I_{IHSCK}	SCK Input Current “H”	V_{DD}=SCK=4.8V	-1		1	μA
I_{ILSCK}	SCK Input Current “L”	V_{DD}=4.8V, SCK=GND	-1		1	μA
R_{PU}	CE Pull-up Resistance		2	4	10	MΩ
I_{CD}	C_D Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
I_{CTW}	C_{TW} Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
$I_{\overline{RESET}}$	$\overline{RESET}$ Pin Output Current	V_{DD}=1.5V, V_{DS}=0.5V	1	2		mA
Ileak	$\overline{RESET}$ Pin Leakage Current	V_{DD}=10.0V, CE=GND, V_{DS}=10.0V	-1		1	μA
T_{SCKW}	SCK Input Pulse Width	V_{DD}=4.8V	500			ns
Vstart	Minimum Operating Voltage of Voltage Detector			0.9	1.5	V

TYPICAL APPLICATION



TECHNICAL NOTES

Use a 0.01μF or more value of an external capacitor, C_W for setting watchdog and reset time-out periods.

Use 1μF or 2.2μF capacitor between V_{DD} and GND, and between V_{OUT} and GND and make its wiring as short as possible.

Make V_{DD} and GND lines sufficient.

Power noise may a cause of incorrect operation of the watchdog timer, because the built-in detector supervises the built-in regulator output, therefore the noise may be detected.

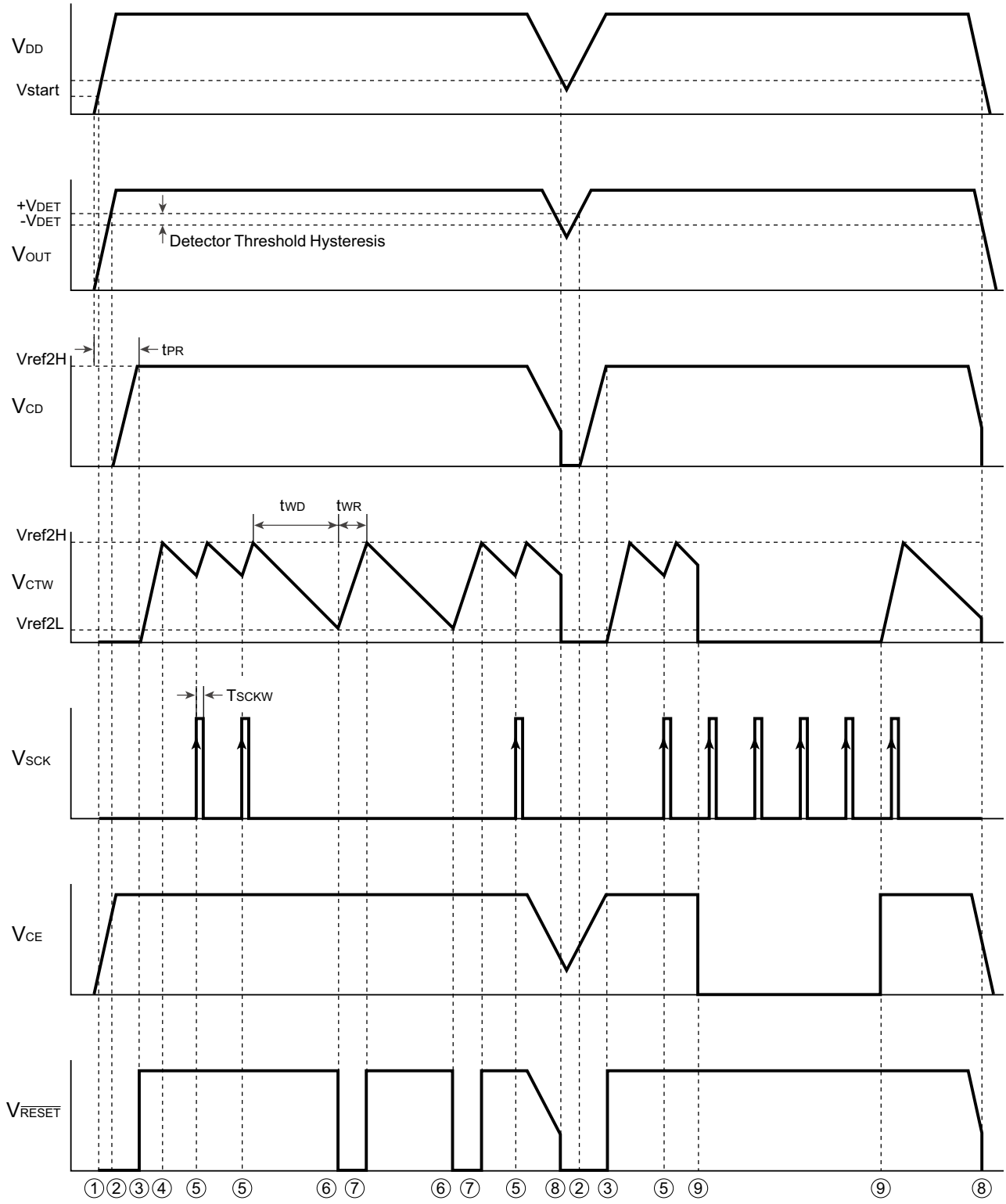
If the capacitance for C_{TW} pin is too large, pick-up noise may be result.

To avoid the mis-operation, during watchdog timer monitoring time, there is some ignoring time against clock pulse. Therefore, during the ignoring time, input clock pulse (rising edge trigger) is ignored. The ignoring time is approximately as follows:

1) The time interval for V_{CTW} pin voltage from $V_{REF}2H$ to ($V_{REF}2H$-$V_{REF}2H/20$)
2) The time interval for V_{CTW} pin voltage from $V_{REF}2L$+$V_{REF}2L/20$ to $V_{REF}2L$

* If an equal or less than 100us-width "L" pulse is input to the CE pin, the error reset may output. The equal or less than 100us width "L" pulse caused by some noise or something against the CE pin must be avoided.

OPERATION DIAGRAM



OPERATION

① When V_{DD} is turned on and Input Voltage reaches Vstart (nearly equal 0.8V), the output of $\overline{RESET}$ pin becomes “L” level.

② An External Capacitor starts to be charged through the C_D pin when an Output Voltage of the Voltage Regulator, V_{OUT}, crosses the Released Voltage, $+V_{DET}$, from Lower to Higher. The $V_{\overline{RESET}}$ is kept “L” level until Voltage of the C_D pin, V_{CD}, reaches to the Vref2H, about 1.0V, and after that the $V_{\overline{RESET}}$ becomes to “H” level.

∗ t_{PR}: Time interval between the timing of starting edge of forcing voltage to V_{DD} pin and the timing of reverse the voltage level of $V_{\overline{RESET}}$.

t_{PR} can be set by connecting an external capacitor to C_D pin, t_{PR} can be calculated as shown below; t_{PR}(ms) ≈ 13000× C_D (μF); C_D means a value of an external capacitor connected to C_D pin.

③ When the voltage level of V_{CD} reaches to the Vref2H, the external capacitor starts to be charged through the C_{TW} pin and the watchdog timer begins to operate.

④ The operation mode for the external capacitor changes from charging mode to discharging mode through C_{TW} pin when the voltage level of C_{TW} pin, V_{CTW}, reaches to the Vref2H.

⑤ While the C_{TW} pin is on the discharging mode, if a clock pulse is entered (synchronous with a rising edge of the pulse), the operation mode of C_{TW} pin changes from discharging mode to charging mode. And the external capacitor connected to C_{TW} pin is charged until its voltage level reaches to Vref2H.

⑥ While the C_{TW} pin is on the discharging mode, if V_{CTW} level drops to Vref2L, about 0.2V without clock pulse to CLK pin, the voltage level of Reset pin becomes from “H” to “L”.

∗ Watchdog Timeout period, t_{WD},: Discharging Time of C_{TW} pin level from Vref2H to Vref2L

t_{WD} can be set by connecting an external capacitor to C_W pin, t_{WD} can be calculated as shown below; t_{WD} (ms) ≈ 10000× C_W (μF); C_W means a value of an external capacitor connected to C_W pin.

⑦ C_{TW} pin is changed to charging mode from discharging mode when the Reset signal is generated.

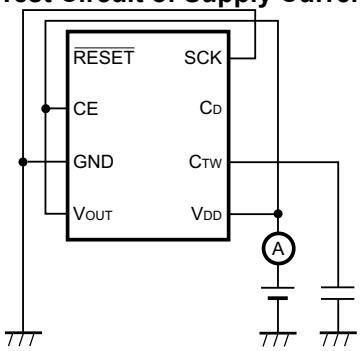
∗ Reset timeout period of the watchdog timer, t_{WR},: Time interval between Charging time of the C_{TW} pin from Vref2L to Vref2H. t_{WR} can be calculated by the next equation as shown below; t_{WR} (ms) ≈ t_{WD}/10

⑧ The Output Voltage level of $\overline{RESET}$ pin becomes from “H” to “L”, or a Reset signal is generated when an output voltage of the Voltage Regulator drops to a level at equal or less than $-V_{DET}$.

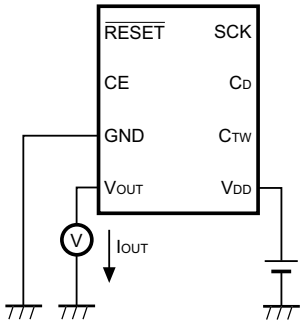
⑨ The watchdog timer will be halted when a Voltage level of CE pin becomes to “L”. In this case, only the watchdog timer is stopped and monitoring the output voltage is continued. After that, if the voltage level of CE pin becomes to “H”, C_{TW} pin starts to be on charging mode.

TEST CIRCUITS

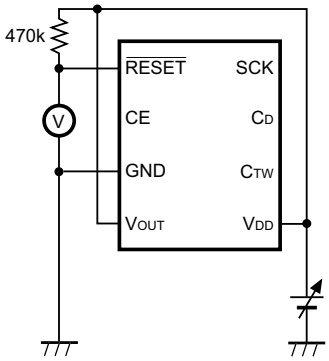
Test Circuit of Supply Current



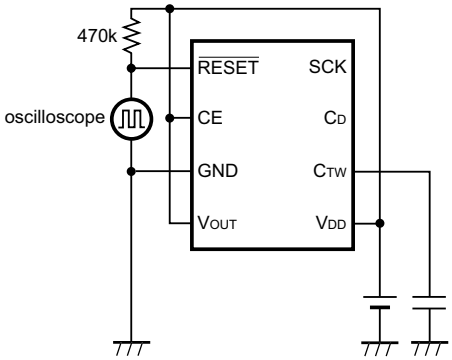
Test Circuit of Output Voltage



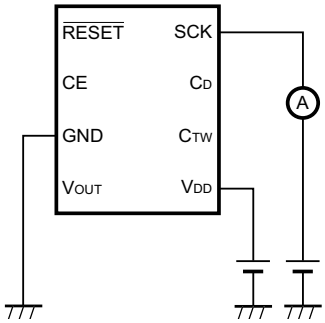
Test Circuit of Detector Threshold(V_{DET})



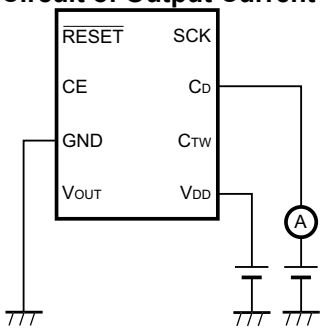
Test Circuit of Reset and Watchdog Timeout Periods



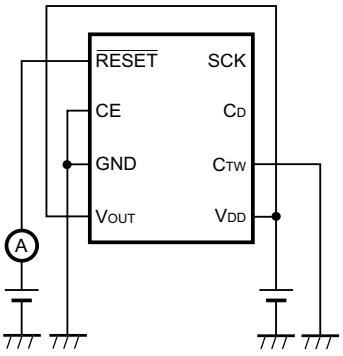
Test Circuit of SCK Input Current



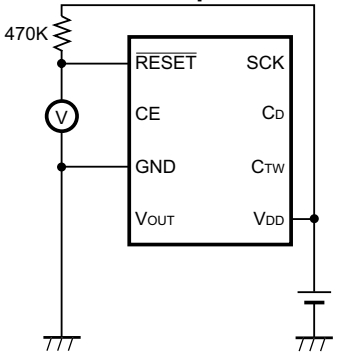
Test Circuit of Output Current



Test Circuit of RESET Output leakage Current



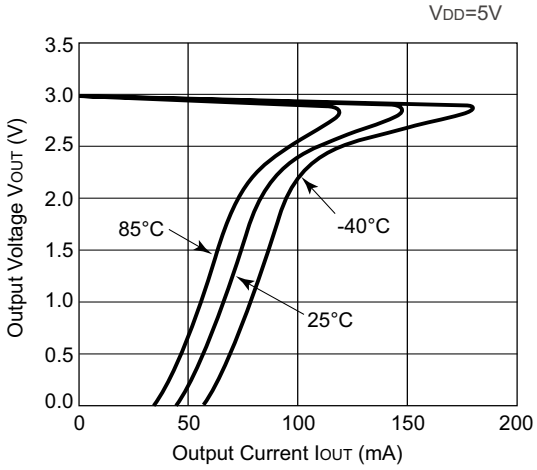
Test Circuit of Minimum Input Voltage for RESET Output



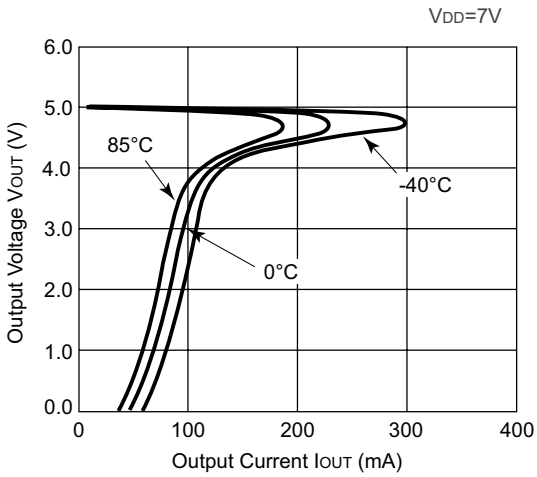
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current

R5101G001A

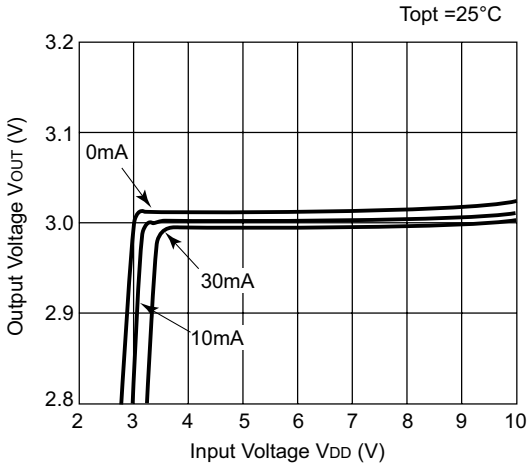


R5101G003,004A

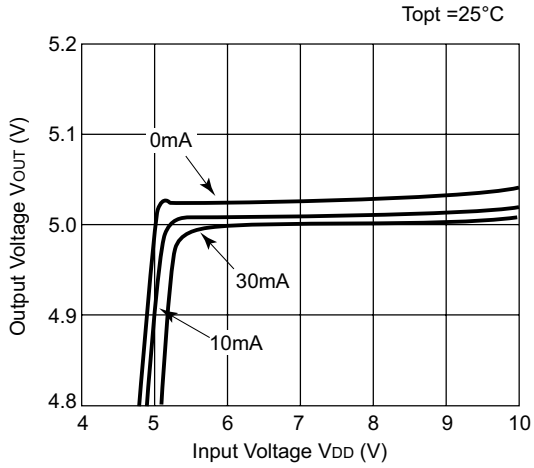


2) Output Voltage vs. Input Voltage

R5101G001A

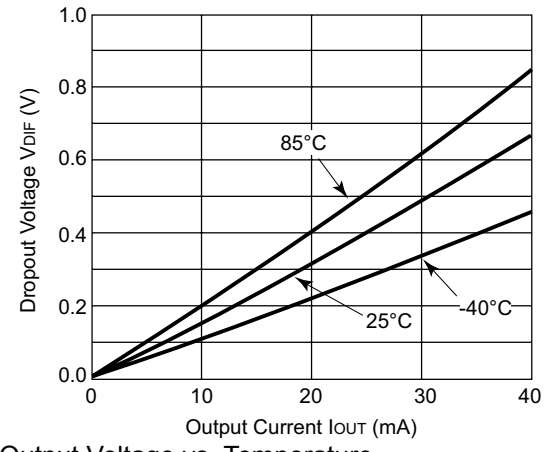


R5101G003,004A

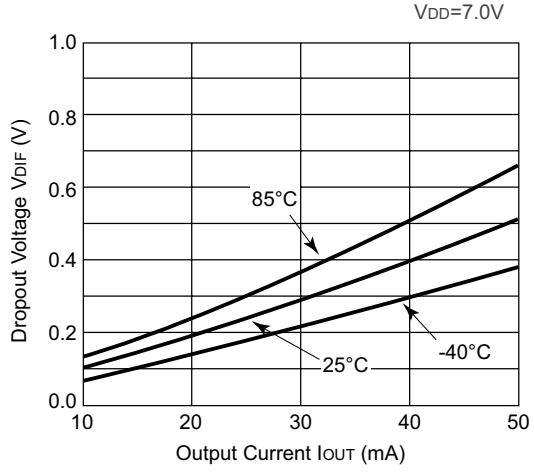


3) Dropout Voltage vs. Output Current

R5101G001A



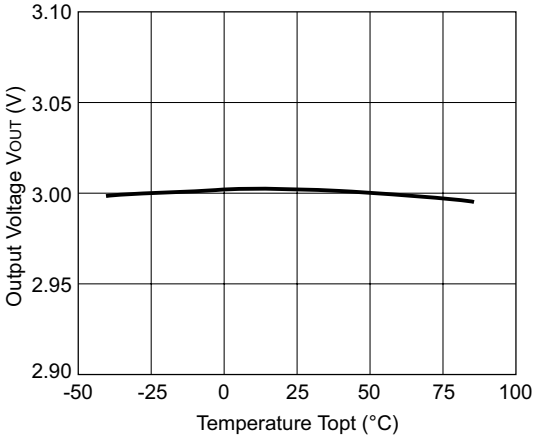
R5101G003,004A



4) Output Voltage vs. Temperature

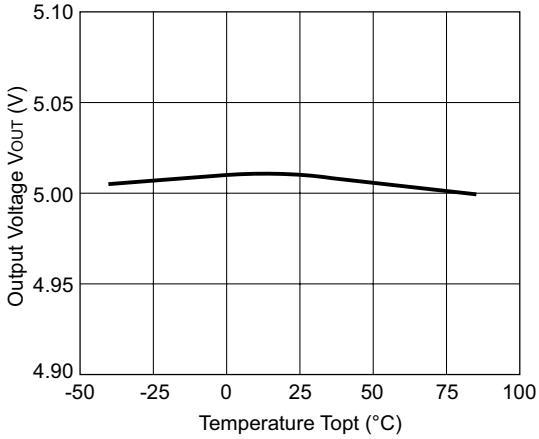
R5101G001A

V_{DD}=5V



R5101G003,004A

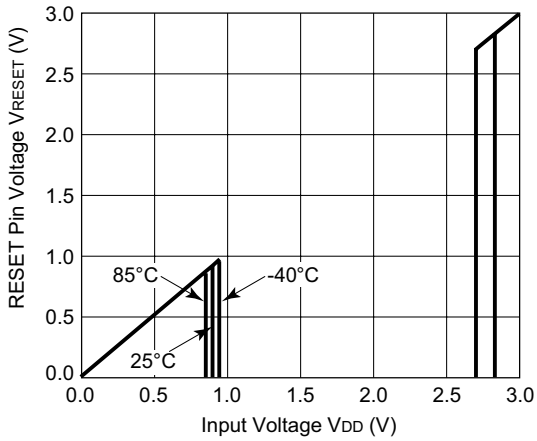
V_{DD}=7.0V, I_{OUT}=10mA



5) RESET Pin Voltage vs. Input Voltage

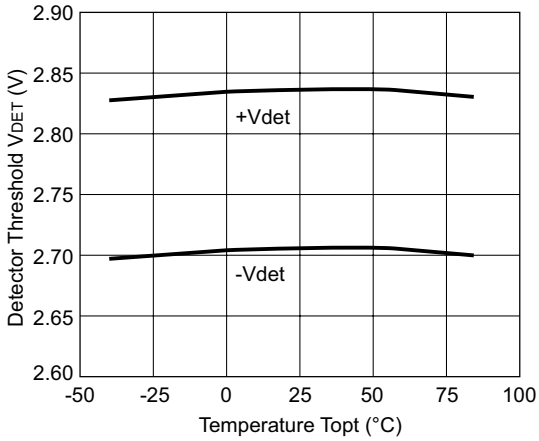
R5101G001A

Pull-up 510kΩ



6) Detector Threshold vs. Temperature

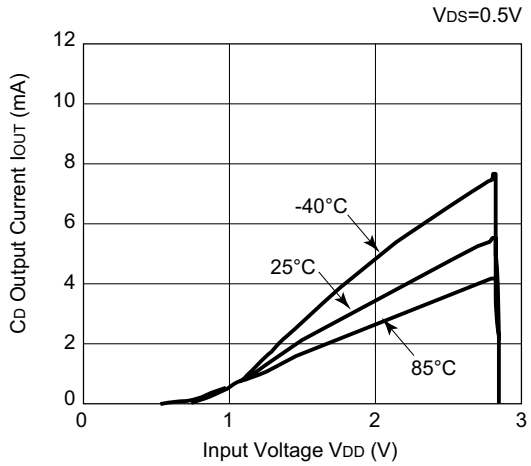
R5101G001A



7) C_D Pin Output Current vs. Input Voltage

R5101G001A

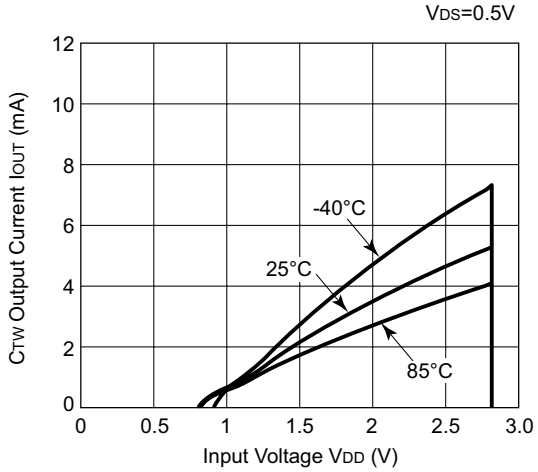
V_{DS}=0.5V



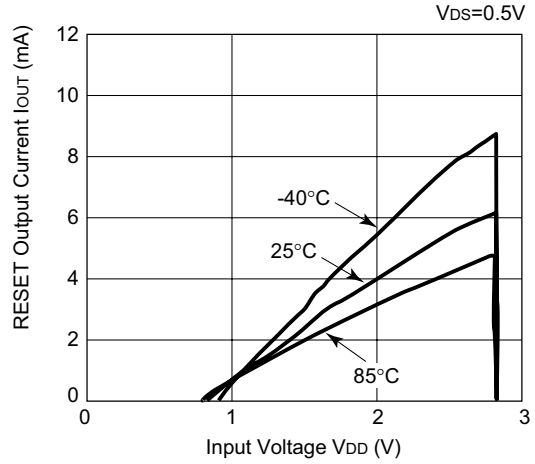
8) C_{TW} Pin Output Current vs. Input Voltage

R5101G001A

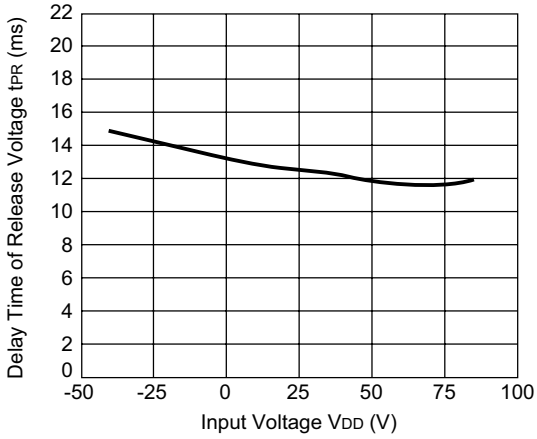
V_{DS}=0.5V



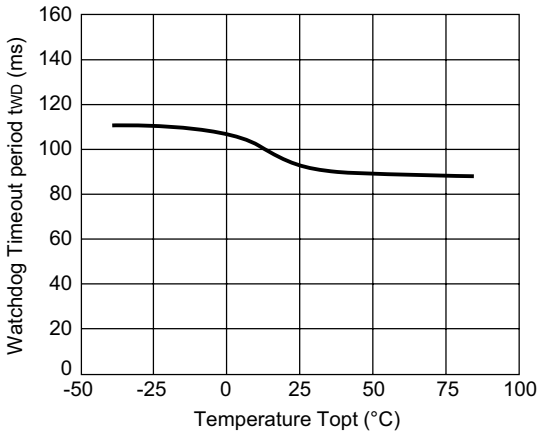
9) RESET Pin Output Current vs. Input Voltage
R5101G001A



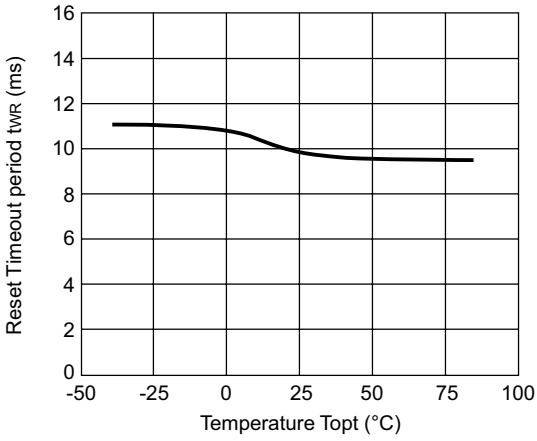
10) Delay Time of Released Voltage vs. Temperature
R5101G001A



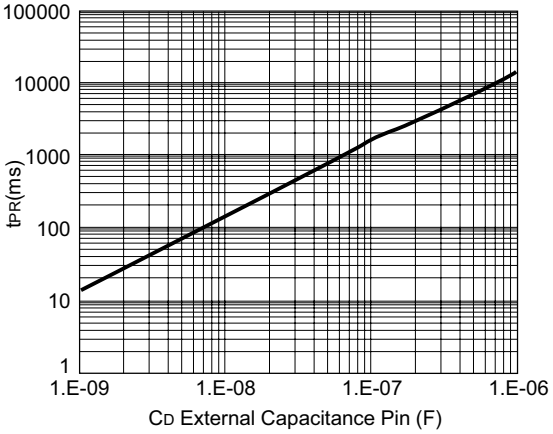
11) Watchdog Timeout period vs. Temperature
R5101G001A



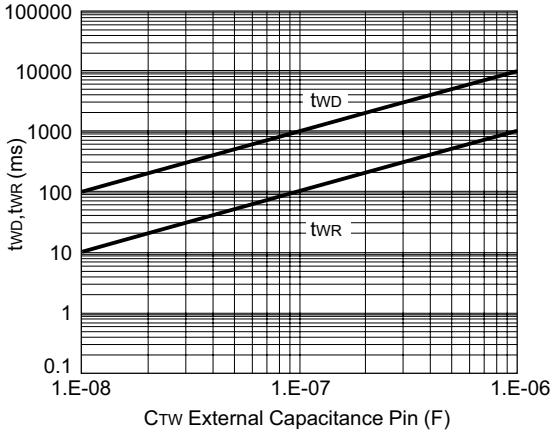
12) Reset Timeout period vs. Temperature
R5101G001A



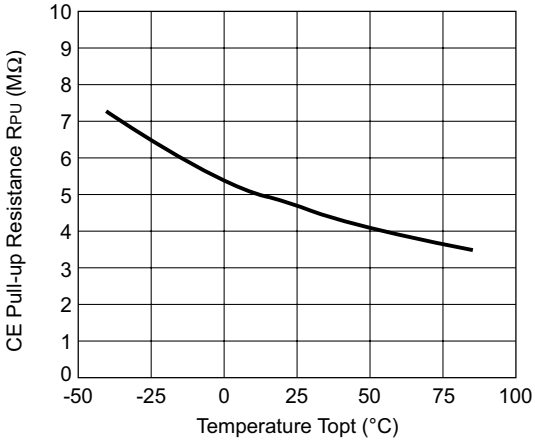
13) t_{PR} vs. External Capacitance of C_D Pin
R5101G001A



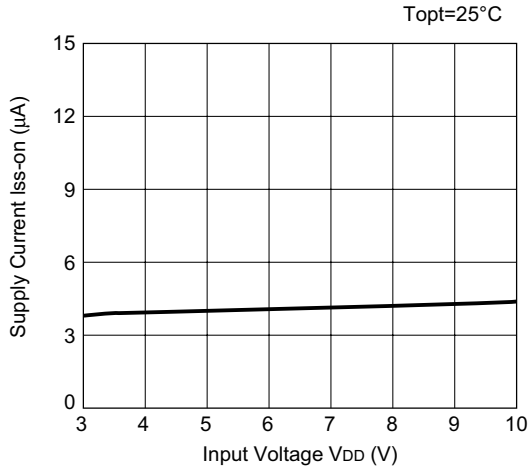
14) t_{WD}, t_{WR} vs. External Capacitance of C_{TW} Pin
R5101G001A



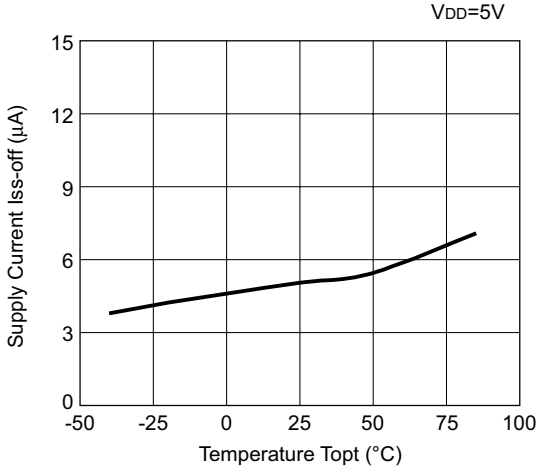
15) CE Pull-up Resistance vs. Temperature
R5101G001A



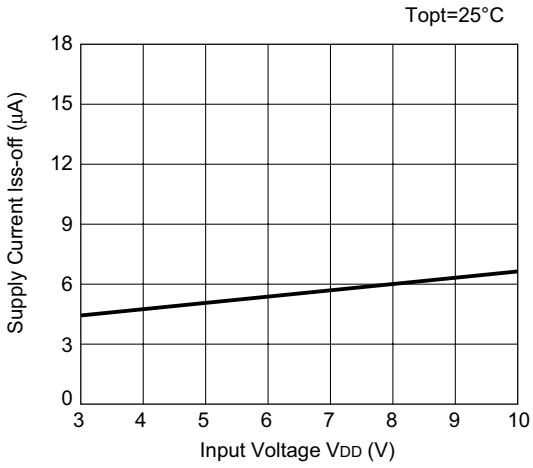
16) Supply Current vs. Input Voltage (W_{DT} ON)
R5101G001A



17) Supply Current vs. Temperature (W_{DT} ON)
R5101G001A



18) Supply Current vs. Input Voltage (W_{DT} OFF)
R5101G001A



19) Supply Current vs. Temperature (W_{DT} OFF)
R5101G001A