

Power Switch IC for Express Card

■ OUTLINE

The R5535V is the power interface switch IC for single slot ExpressCard and realizes the total power management function required by ExpressCard. The R5535V distributes 3.3V, 3.3Vaux, and 1.5V to the ExpressCard socket. Each voltage line is protected with a built-in current limit circuit and a thermal shutdown circuit in the R5535V.

■ FEATURES

- Meets the Express Card™ Standard
- Built-in Over-current Limit
- Built-in Clock Enable Function
- With 3.3VIN and 3.3V AUXIN Sequence
- Package SSOP-20

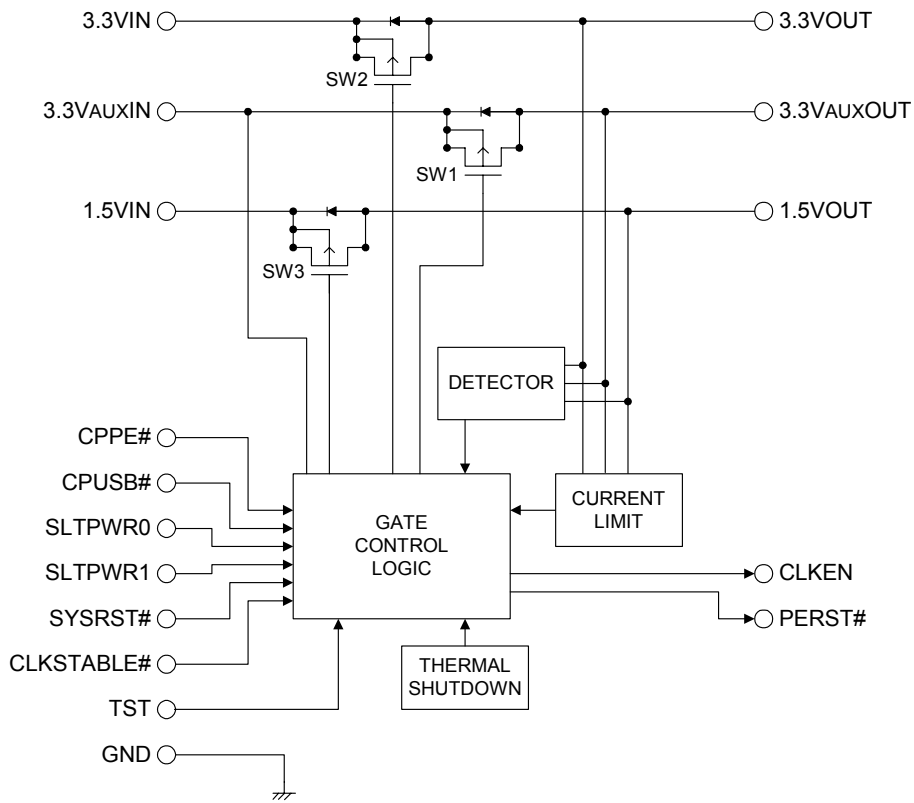
■ PIN CONFIGURATION (Top view)

SLTPWR0	□	1	○	20	□	CPUSB#
SLTPWR1	□	2		19	□	CPPE#
SYSRST#	□	3		18	□	CLKSTABLE#
1.5VIN	□	4		17	□	1.5VOUT
1.5VIN	□	5		16	□	1.5VOUT
3.3VIN	□	6		15	□	3.3VOUT
3.3VIN	□	7		14	□	3.3VOUT
3.3VAUXIN	□	8		13	□	CLKEN
GND	□	9		12	□	PERST#
3.3VAUXOUT	□	10		11	□	TST

*Same name pins should be connected one another.

*TST pin should be connected to the GND.

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Symbol	Pin description
3.3VAUXIN	3.3VAUX Input Pin
3.3VIN	3.3V Input Pin
1.5VIN	1.5V Input Pin
GND	Ground Pin
CPPE#	Logic Input Pin
CPUSB#	Logic Input Pin
SLTPWR0	Logic Input Pin
SLTPWR1	Logic Input Pin
SYSRST#	Logic Input Pin
CLKSTABLE#	Logic Input Pin
3.3VOUT	3.3V Output Pin
3.3VAUXOUT	3.3VAUX Output Pin
1.5VOUT	1.5V Output Pin
PERST#	Logic Output Pin
CLKEN	Logic Output Pin
TST	Test Input Pin

■ ABSOLUTE MAXIMUM RATINGS

GND=0V

Item	Symbol	Ratings	Unit
Input Voltage (3.3V _{AUX})	3.3V _{AUXIN}	-0.3 to 5.0	V
Input Voltage (3.3V)	3.3V _{IN}	-0.3 to 5.0	V
Input Voltage (1.5V)	1.5V _{IN}	-0.3 to 2.5	V
Logic Input Voltage	V _{IN}	-0.3 to 5.0	V
TST Input Voltage	VTST	-0.3 to 5.0	V
Logic Output current	I _{LOGICOUT}	-1 to 4	mA
Output Current	I _{3.3VOUT}	>1.3A Internal Limited	
	I _{3.3VAUXOUT}	>400mA Internal Limited	
	I _{1.5VOUT}	>650mA Internal Limited	
Power Dissipation	P _D	Internal Limited	
Operating Temperature Range	T _{opt}	-40 to 85	°C
Storage Temperature Range	T _{stg}	-55 to 125	°C

[Note] Absolute maximum ratings are threshold limit values that must not be exceeded even for any moment under any conditions. More over, such values for any two or more items of the ratings must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or fatal damage to the device. These mean stress ratings and do not necessarily imply functional operation below these limits.

ELECTRICAL CHARACTERISTICS

T_{opt}=25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage(3.3V _{AUX})	3.3V _{AUXIN}		3.0	3.3	3.6	V
Supply Voltage(3.3V _{IN})	3.3V _{IN}		3.0	3.3	3.6	V
Supply Voltage(1.5V)	1.5V _{IN}		1.35	1.50	1.65	V
Supply Current	I _{CCAUX}	Output pins: Open		45	90	μA
	I _{SIPAUX}	Sleep Mode, Output=0V		0.3	10	μA
	I _{CC3.3V}	Output pins: Open		15	30	μA
	I _{SIP3.3V}	Sleep mode, Output=0V		0.2	10.0	μA
	I _{CC1.5V}	Output pins: Open		15	30	μA
	I _{SIP1.5V}	Sleep mode, Output=0V		0.5	70.0	μA
3.3V _{OUT} switch resistance	R _{o3.3V}	3.3V _{IN} =3.3V, I _{OUT} =1.3A		65		mΩ
		Select 3.3V _{OUT} =0V		500	3900	Ω
3.3V _{AUXOUT} switch resistance	R _{o3.3V_{AUX}}	3.3V _{AUXIN} =3.3V, I _{OUT} =400mA		170		mΩ
		Select 3.3V _{AUXOUT} =0V		500	3900	Ω
1.5V _{OUT} switch resistance	R _{o1.5V}	1.5V _{IN} =1.5V, I _{OUT} =650mA		70		mΩ
		Select 1.5V _{OUT} =0V		500	3900	Ω
Short Current Limit	I _{B.3VSC}	3.3V _{OUT} =0V	1.3	2.0		A
	I _{B.3V_{AUX}SC}	3.3V _{AUXOUT} = 0V	0.4	0.7		A
	I _{B.1.5VSC}	1.5V _{OUT} =0V	0.65	1.00		A
Logic Input "H" Voltage	V _{IH}		2.0		3.9	V
Logic Input "L" Voltage	V _{IL}		-0.3		0.8	V
Logic Input Current	I _{IN}	0V < V _{IN} < 3.6V	-1		1	μA
Logic Output "H" Voltage	V _{OH}	I _{OH} =-500μA	2.6			V
Logic Output "L" Voltage	V _{OL}	I _{OL} = 2mA			0.4	V
Thermal Shutdown Temperature	T _{SD}			135		°C
3.3V _{OUT} Detector Threshold Voltage	V _{DET3.3}	At 3.3V Output falling	2.50	2.75	3.00	V
3.3V _{AUX} Detector Threshold Voltage	V _{DETAUX}	At 3.3V _{AUX} Output falling	2.50	2.75	3.00	V
1.5V _{OUT} Detector Threshold Voltage	V _{DET1.5}	At 1.5V _{OUT} Output falling	1.20	1.27	1.35	V

Topt=25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
3.3VAUXOUT Turn-on Delay Time	t 1	3.3VAUXOUT=0V to 10% of 3.3V		0.2	10.0	ms
3.3VOUT Turn-on Delay Time	t 2	3.3VOUT=90% of 3.3VAUXOUT to 10% of 3.3VOUT	1	3	20	ms
1.5VOUT Turn-on Delay Time	t 3	1.5VOUT=0V to 10% of 1.5V		1.8	10.0	ms
3.3VAUXOUT Rising Time	t 4	3.3VAUXOUT=10% to 90% of 3.3V	0.1	1.0	10.0	ms
3.3VOUT Rising Time	t 5	3.3VOUT=10% to 90% of 3.3V	0.1	1.5	10.0	ms
1.5VOUT Rising Time	t 6	1.5VOUT=10% to 90% of 1.5V	0.1	1.0	20.0	ms
3.3VAUXOUT Turn-off Delay Time	t 7	3.3VAUXOUT=10% of 3.3VOUT to Hi-Z of 3.3VAUXOUT	1	3	20	ms
3.3VOUT Turn-off Delay Time	t 8	3.3VOUT=3.3V to Hi-Z		3	20	ms
1.5VOUT Turn-off Delay Time	t 9	1.5VOUT=1.5V to Hi-Z		3	20	ms
3.3VAUXOUT Falling Time	t 10	3.3VAUXOUT=90% to 10% of 3.3V	0.1	0.6	10.0	ms
3.3VOUT Falling Time	t 11	3.3VOUT=90% to 10% of 3.3V	0.1	0.6	10.0	ms
1.5VOUT Falling Time	t 12	1.5VOUT=90% to 10% of 1.5V	0.1	1.0	20.0	ms
PERST# Rising Delay Time against OUT="On"	t 20	From all output voltage reaches each spec to the rising edge of PERST#	1.0	2.5	10.0	ms
PERST# Falling Delay Time against OUT="Off" or Reset State	t 21	From changing the logic input to falling edge of PERST#		1	10	μs
PERST# Delay Time against SYSRST# rising edge	t 22		110	400	1200	μs
PERST# Delay Time against OUT="Fail"	t 23	From falling an output down to out of spec, to falling edge of PERST#		250	500	ns
PERST# "L" period	t 24		100	400	1200	μs
CLKEN Rising Delay Time	t 25			1	10	μs
CLKEN Falling Delay Time	t 26		20	60	200	μs
PERST# Rising Delay Time against CLKSTABLE# Falling Edge	t 27		100	400	1200	μs
PERST# Falling Delay Time against CLKSTABLE# Rising Edge	t 28			1	10	μs

(*Note 1) t2,t3,t5,t6,t8,t9,t11,t12: Test Condition: RL=10Ω

(*Note 2) t1,t4,t7,t10: Test Condition: RL=40Ω

(*Note3) Do not apply to current limit or thermal shutdown conditions during t7, t8, and t9.

(*Note4) t20, t21, t22, t23, t24, t25, t26, t27, t28: Test Condition: CL=100pF

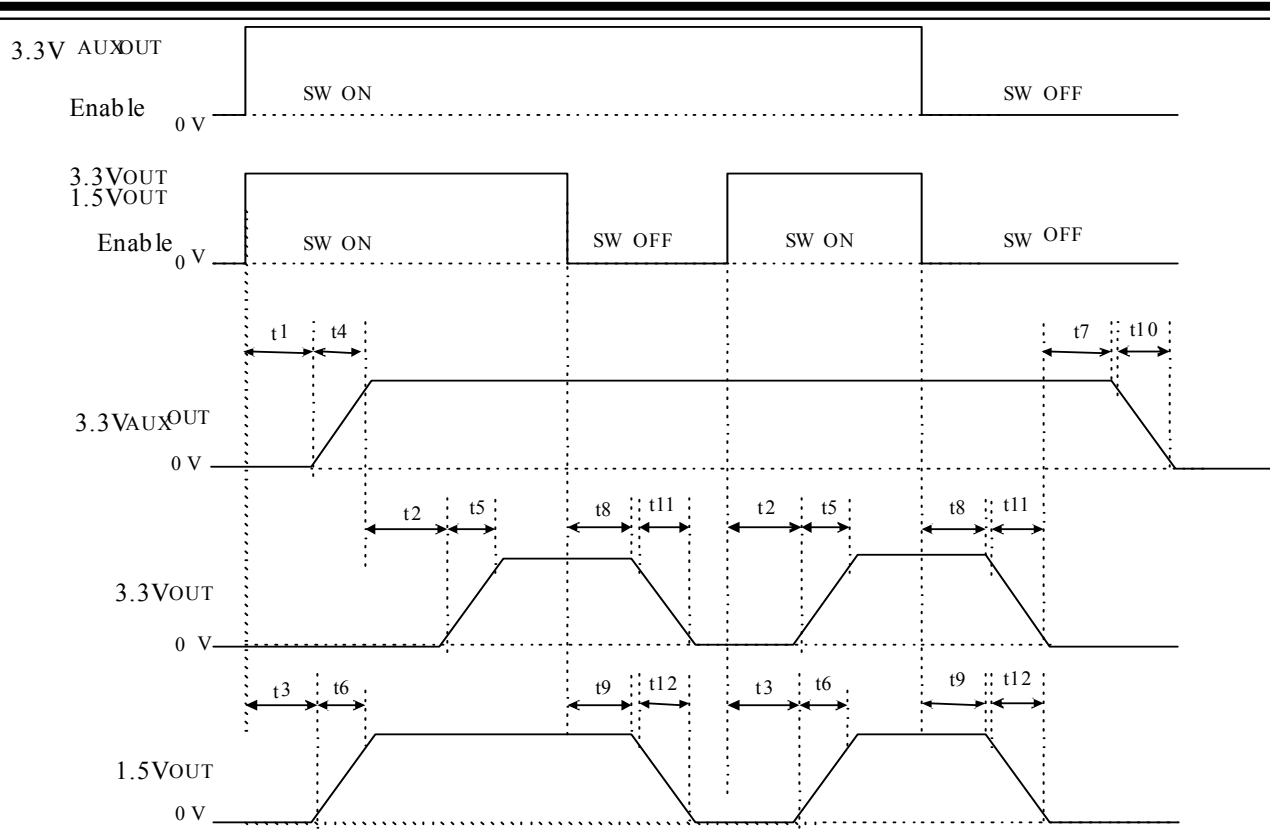


Figure 1. OUT Timing Chart

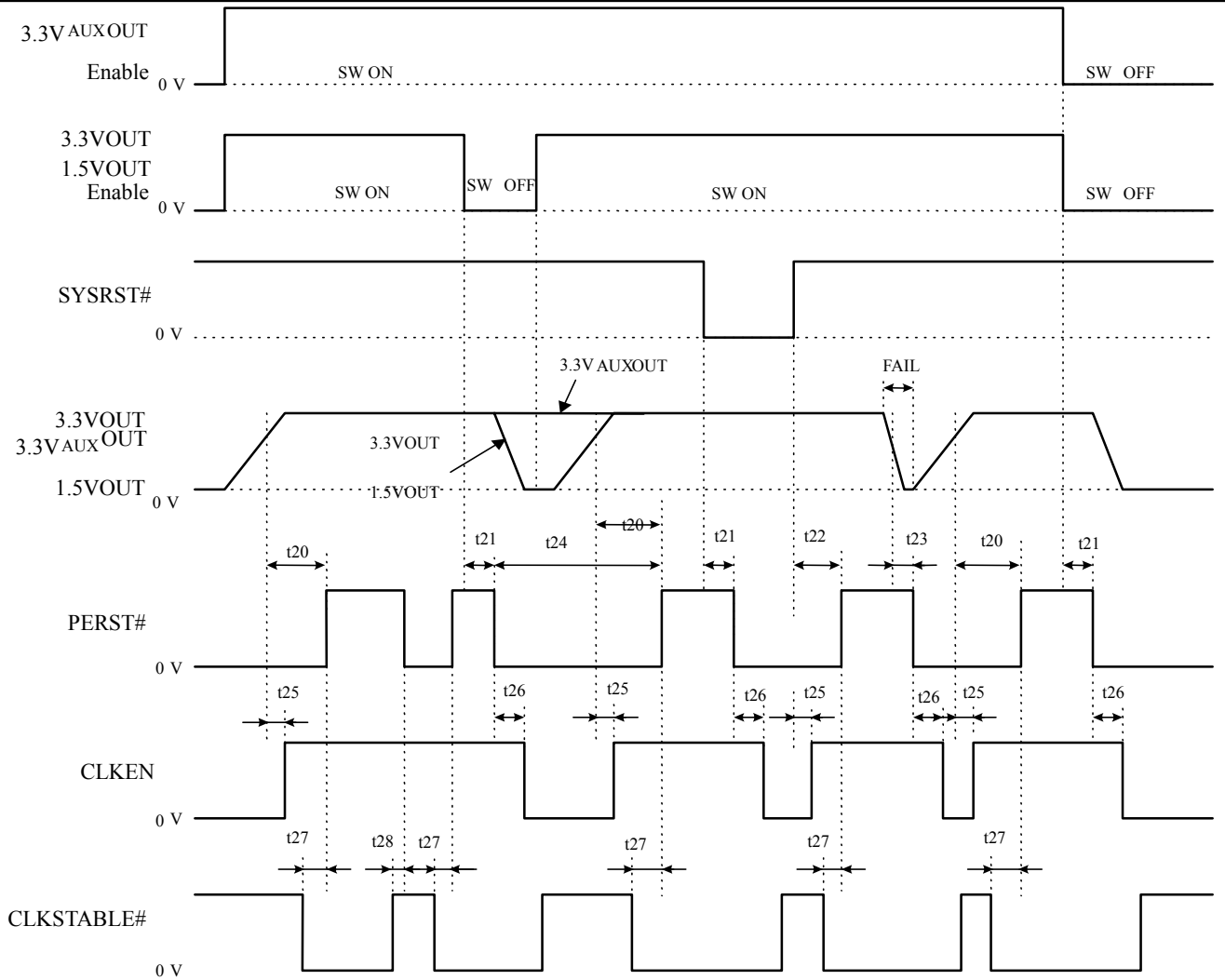


Fig. 2 PERST#, CLKEN, CLKSTABLE# Timing Chart

R5535 Control Logic Table

System Power State		CPUSB#	CPPE#	3.3V _{AUX} OUT	3.3VOUT	1.5VOUT
SLTPWR1 (Primary)	SLTPWR0 (Auxiliary)					
0	0	X	X	0V	0V	0V
1	1	1	1	0V	0V	0V
1	1	1	0	3.3V	3.3V	1.5V
1	1	0	1	3.3V	3.3V	1.5V
1	1	0	0	3.3V	3.3V	1.5V
0	1	1	1	0V	0V	0V
0	1	1(*Note1)	0(*Note1)	3.3V	0V	0V
0	1	0(*Note1)	1(*Note1)	3.3V	0V	0V
0	1	0(*Note1)	0(*Note1)	3.3V	0V	0V
0	1	1(*Note2)	0(*Note2)	0V	0V	0V
0	1	0(*Note2)	1(*Note2)	0V	0V	0V
0	1	0(*Note2)	0(*Note2)	0V	0V	0V
1	0	X	X	0V	0V	0V

X: 1 or 0

(*Note 1) In case that CPUSB# and CPPE# are asserted before this system power state.

(*Note 2) Even if CPUSB# or CPPE# are asserted after this system power state, each output keeps the change off the previous state.

OPERATION

When both SLTPWR0 and SLTPWR1 are "0", the IC enters the sleep state, and consumption current is decreased to 1.0 μ A (Typ.).

If OUT is shorted to GND, and the over-current limit continues, the IC temperature is rising. If the IC temperature inside is beyond 135°C(Typ.), then the switch transistor is off. Then, when the IC temperature decreases by 10°C from the point, the switch transistor is on again. Unless the cause of the over-current is removed or switch is disabled, the switch transistor repeats on and off.

The short current limit is set internally in this IC. There are two cases for the response at the over-current.

(Case 1) If OUT pin is short or connected to a very large load and the switch is enabled, the switch enters the constant current mode immediately. The current value at the constant current mode is the short current limit value.

(Case 2) If the switch transistor is on and OUT is short or connected to a very large load, a large transient current flows until the current limit circuit responds. The transient current depends on the impedance between the voltage suppliers of this IC and the output loading, in other words, the voltage supplier's transient characteristic, the PCB layout, and the card connector. After the current limit circuit responds, the IC enters the constant current state, and the current level is specified as the short current limit value.

If CPPE#="1", then PERST#="0".

The rising delay time of PERST# depends on the longest time among t20, t22, and t27. For example, if the rising edge of CLKEN is synchronized with the falling edge of CLKSTABLE#, $t25+t27 < t20$ is true, therefore, the rising delay time of PERST# is determined as t20.

If 3.3VOUT=0V, then 3.3VIN can be turned off.

APPLICATION NOTES

* Same name pins should be connected one another.

* There is a parasitic diode between source and drain of the switch transistors. (Refer to the block diagram.) Therefore, even if the switch may be disabled, in case the OUT voltage is higher than the power supply voltage, some current flows from OUT to the input side.

* Connect TST to the GND.

*3.3VIN and 3.3VAUXIN can be connected.