酸化物半導体を用いた全印刷薄膜トランジスタアレイの開発

All-Printed Oxide Thin Film Transistor Arrays for High Resolution Active Matrix

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要　旨

インクジェット法とスピンコート法を用いて，酸化物半導体を活性層に用いた100ppi RGBアクティブマトリックスの薄膜トランジスタアレイをマスクレスで製造するプロセスを開発した．熱酸化膜付シリコン基板上に製造したTFTは，平均電界効果移動度7.49cm^2/Vsを示した．また，ドーピングによる活性層のキャリア制御を検討し，特性ばらつきの少ない酸化物TFTアレイが製造できることを示した．さらに，新規の高誘電率酸化物絶縁体をゲート絶縁膜に用いた全印刷TFTは，平均電界効果移動度2.54cm^2/Vsを示した．全印刷プロセスによって，ノーマリーオフの特性と立ち上がり電圧の揃った酸化物TFTアレイが実現できることを示した．

ABSTRACT

We have demonstrated oxide TFT arrays for 100 ppi RGB active matrix fabricated by inkjet printing and spin coating without photolithography and mask process. The average mobility of TFTs was 7.49 cm^2/Vs on a thermally oxidized SiO_2 /Si substrate. We have also shown the method of controlling the carrier generation by n-type doping technique and the printed oxide TFT arrays with small variation properties were obtained. Moreover, in the result of combination a novel oxide high-k gate insulator and the n-type doping to active layer, all-printed oxide TFTs on a glass substrate exhibited the average mobility of 2.54 cm^2/Vs. Normally-off operation and excellent small variation of the turn-on voltage were obtained by the all printing processes.

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1. Background

In recent years, researches of printing fabrication technologies for electronics devices are activating. Especially, direct patterning process like an inkjet printing attracts big attention as the resource and energy saving process. Compared to conventional photolithography and mask process which have been used as manufacturing of today's display panels, it has several advantages such as scalability to variable substrate size and small initial investment for manufacturing facilities, then it can realize on-demand, wide variety and variable quantities productions. Therefore direct printing fabrication without mask process is an expected manufacturing technology in future.

After Nomura et al. disclosed a thin film transistor (TFT) using amorphous $InGaZnO_4$ (a-IGZO) [1], numerous studies on oxide semiconductor TFTs have been extensively carried out. Because of several advantages to amorphous silicon TFTs and polycrystalline silicon TFTs such as high uniformity and stability of device performance and small off-current level, oxide TFTs have become the main candidate of backplane for large size and high resolution display panels. In fact, the 32 inch active matrix LCD device with 4K/2K resolution (140 ppi) has become commercially available made by traditional process with photolithography and vacuum film formation.

In addition, there are many reports about solution processed oxide TFTs aimed at the resource, energy and cost saving processes. So far, IGZO [2], IZO [3,4], and In_2O_3 based films [5], which were fabricated by solution process such as spin coating, were used as active layers of oxide TFTs and the high field effect mobility were obtained.

However, in fabrication of the oxide TFT and the active matrix device by using printing technique, there are many requirements for materials on each layer such as the gate and source-drain electrodes, gate insulator, and semiconductor. Moreover, all-printed fabrication requires consistency against every process such as printing and heating of each layer from gate to semiconductor. Therefore in the previous reports about solution processed oxide TFTs, photolithography and/or mask processes have been used for patterning of the source-drain electrodes and/or the semiconductor layers. So there are no reports about all-printed process of oxide TFTs.

Recently we have reported the method of controlling the carrier generation by substitutional doping technique in $MgIn_2O_4$ TFT [6] and fabrication of the printed oxide high-k gate insulators for oxide TFTs [7]. Building on the technologies we have demonstrated all-printed oxide TFT arrays for 100 ppi RGB active matrix fabricated by inkjet printing and spin coating in this paper.

2. Experimental Details and Results

2-1 Fabrication of Gate Layer

For TFT fabrication we adopted bottom-gate and bottom-contacts geometry. Because of endurance against high temperature and low resistivity, the gate layer was manufactured from Au nano-particle ink by inkjet printing on a glass substrate. The baking temperature was 250 °C.

Figure 1 shows a photograph of the gate layer for 100 ppi RGB active matrix with 2T1C circuits.

The sub-pixel size and number are 85 x 255 μm and 18 x 9 arrays, respectively. The typical line width and thickness were 10 μm and 90 nm, respectively. The resistivity was evaluated by 2 wire method and typically 10 μΩcm, which value was enough low for the gate electrodes.

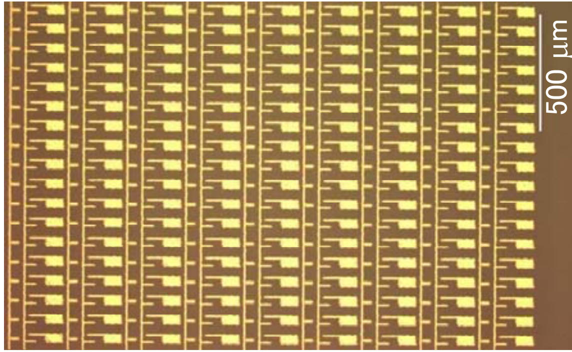

Fig.1 Photograph of 100 ppi 2T1C gate layer manufactured from Au nano-particle ink.

2-2 Fabrication of SD and OSC Layer

To evaluate electrical properties of printed oxide TFTs, whose source and drain (SD) electrodes and oxide semiconductor (OSC) layer were patterned by inkjet printing, we fabricated SD layer and OSC layer on a thermally oxidized SiO_2/Si substrate. For the SD layer, we choose ITO electrode, which is expected to form excellent electrical contact with oxide semiconductor. ITO nano-particle ink was used as the SD ink. The maximum baking temperature was 400 °C. The typical line width and thickness were 10 μm and 100 nm, respectively. For fundamental evaluations of transistor characteristics, the small contact pads were patterned near the channel region. The channel width and length (W/L) were defined by the SD electrodes and measured by using optical microscope. The typical W/L was 30/10 μm.

Next, the OSC layer was formed on the channel regions by inkjet printing. An indium strontium oxide based oxide semiconductor was adopted for the TFTs. We prepared two kinds of OSC inks; the ink A was a solution for indium strontium oxide (ISO) and the ink B was that for n-type doped indium strontium oxide. To remove residual solvent and other organic components, a baking process was performed at 400 °C for 1 hr. Post-annealing was carried out at 300 °C for 1 hr to investigate the effect of the heating process for the active layer. Figure 2 shows the photographs of the printed SD electrodes and OSC layers. The inset figure shows the expanded view of the channel region.

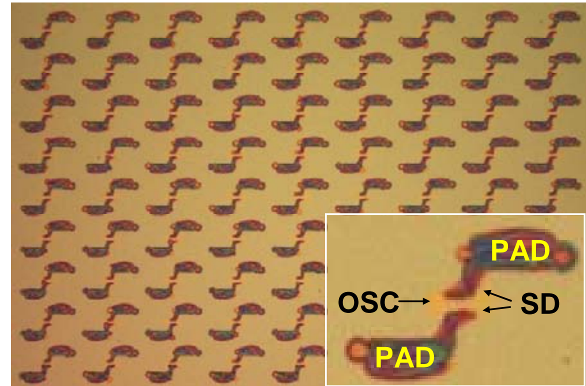

Fig.2 Photographs of ITO SD and OSC layers printed on a Si/SiO_2 substrate.

2-3 TFT Characteristics of N-typed Doped and Non-doped ISO TFT

To evaluate TFT characteristics, the heavily doped Si substrate and the thermally oxidized SiO_2 layer (200 nm thick) served as the gate and the gate insulator, respectively. The TFT properties were measured by Keithley 4200SCS semiconductor characterization system.

Figure 3 shows the I_{DS}-V_{GS} curves of the 76 non-doped ISO TFTs manufactured from ink A, as baked (Fig.3 (a)) and after post-annealing (Fig.3 (b)). The field effect mobility was calculated with conventional metal-oxide-semiconductor field effect transistor model at V_{GS} ~ 20 V. Figure 3 (c) shows the histogram of the mobility for the 76 non-doped ISO TFTs. The TFTs, as baked and after post-annealing, exhibited the mean value in the mobility of 7.94 and 7.49 cm^2/Vs, the threshold voltage Vth of -4.9 and -3.2 V, the S-value of 0.47 and 0.47 V/dec, and the on/off current ratio over 10^8, respectively. The maximum mobility as baked and after post-annealing reaches 10.57 and 10.49 cm^2/Vs, respectively, which values are the top performance in oxide TFTs patterned by inkjet printing.

Figure 4 shows the I_{DS}-V_{GS} curves of the n-type doped ISO TFTs manufactured from ink B, as baked (Fig.4 (a)) and after post-annealing (Fig.4 (b)), and the histogram of the mobility for the 32 TFTs (Fig.4 (c)). The n-type doped ISO TFTs, as baked and after post-annealing, exhibited the mean value in the mobility of 2.46 and 2.66 cm^2/Vs, the threshold voltage Vth of 2.55 and 1.34 V, the S-value of 0.80 and 0.70 V/dec, and the on/off current ratio over 10^8, respectively. Although the average mobility of the n-type doped ISO TFTs is lower than that of the non-doped ones, the standard deviation of the mobility in the doped TFTs is better than that in the non-doped ones both as baked and after post-annealing (Fig.3 (c), 4 (c)). In addition, the standard deviation of the mobility in the n-type doped TFTs tend to decrease under post-annealing process. On the contrary, the non-doped TFTs show an opposite tendency.

One of the reasons that the non-doped ISO TFTs exhibited the large amount of deviation in the mobility both as baked and after post-annealing is presumed the generation or extinction of oxygen vacancy in the active layer. The electron carriers generated by oxygen vacancy mainly contribute to the property of the active layer. So in order to obtain the homogeneous device performance, the amount of oxygen vacancy of the active layer in the TFT array must strictly be controlled, but it seems difficult only by adjusting the heating conditions.

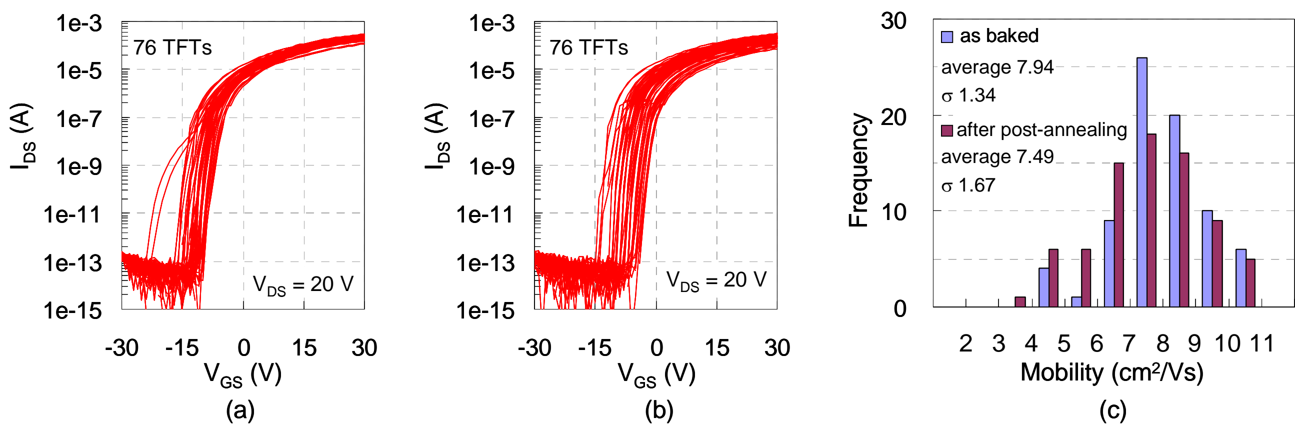

Fig.3 (a) Transfer curves as baked, (b) after post-annealing, (c) the histogram of the mobility for 76 non-doped ISO TFTs.

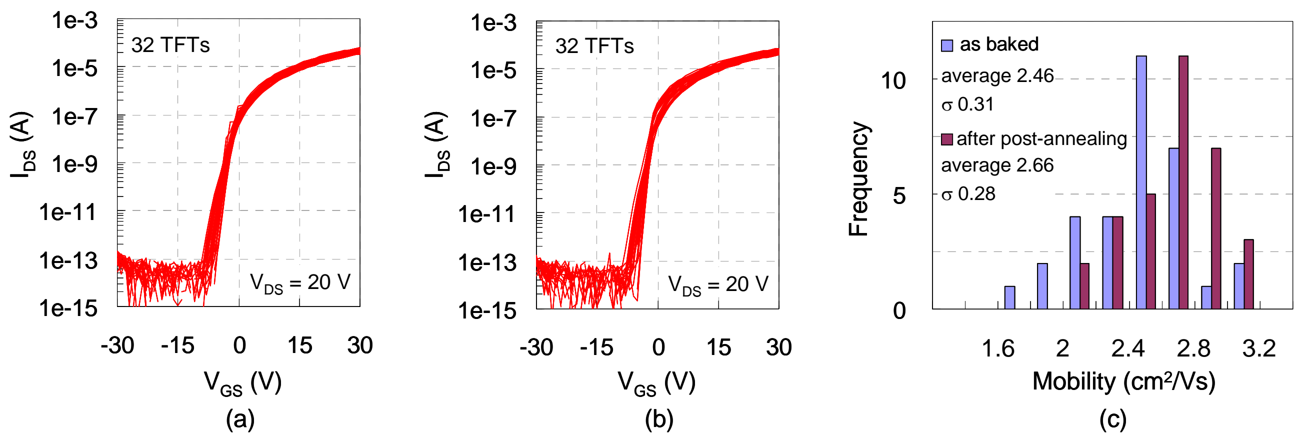

Fig.4 (a) Transfer curves as baked, (b) after post-annealing, (c) the histogram of the mobility for 32 n-type doped ISO TFTs.

On the other hand, in the case of the n-type doped ISO TFTs, electron carriers generated by the doping dominate the property of the active layer, and the oxygen vacancy does not contribute to the device performance. Therefore, the n-type doped ISO TFTs exhibit the better device uniformity as baked and after post-annealing process than the non-doped ones. This result means that the substitutional doping even in the solution process is effective to enlarge the margin of the fabrication processes in the same way of the doped IMO TFT fabricated by the vacuum process as reported before [6].

2-4 Fabrication and Characteristics of Novel Printed Oxide High-k Gate Insulators

As the gate insulator (GI) materials, we selected the novel printed oxide high-k gate insulators (POGI)[7]. The POGI were manufactured from lanthanum alkaline earth oxides (LRO). The inks of POGI were prepared by dissolving 2-ethylhexanoate of lanthanum, magnesium, strontium, and barium in toluene. The atomic ratio of lanthanum by alkaline earth metal was changed from 1 to 11 (denoted by LRO1 to LRO11). Accordingly, colorless, transparent inks for forming LRO films were prepared.

The POGI films were formed by spin coating on glass substrates. Then, a heating process was performed at 120 °C for 1 hr and 400 °C for 3 hrs in air. The thickness of the LRO films was controlled from 150 to 350 nm.

For the dielectric property measurements, we fabricated the capacitor devices, which have a structure of Al/LRO/Al. The aluminum electrodes were formed by vacuum evaporation via a metal mask and the thickness was 100 nm. As a reference, the capacitor device was also fabricated with a SiO_2 insulator film deposited by RF magnetron sputtering method. The capacitor area was 1.0 mm^2. The dielectric properties were measured by 2 wire method using Agilent 4284 LCR meter. Figure 5 and Figure 6 show the frequency dependence of the dielectric constant k and the dielectric loss (tan δ) of the spin-coated LRO. As a reference, the data of the RF magnetron sputtered SiO_2 film are also shown in the figures. The SiO_2 film showed the k of 3.9 which value is equal to that of the thermally oxidized SiO_2 film and the very low tan δ over all frequency range. For LMO1 (La/Mg=1), LSO2 (La/Sr=2), LBO8 (La/Ba=8), and LSXO, which were added a little modification to LSO2, the k at 1 kHz was 6.5, 9.9, 12.2, and 12.8 respectively. Tan δ of these samples was low enough for the actual application less than 0.02 under 100 kHz.

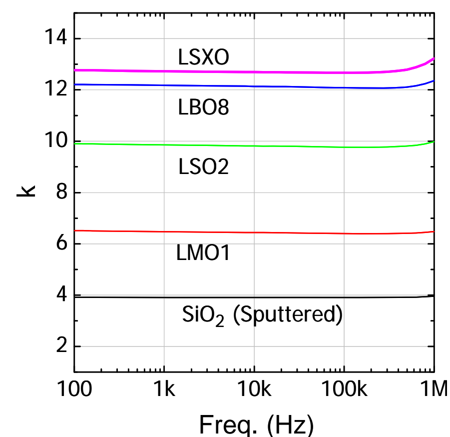

Fig.5 Frequency dependence of the dielectric constant k for POGI films.

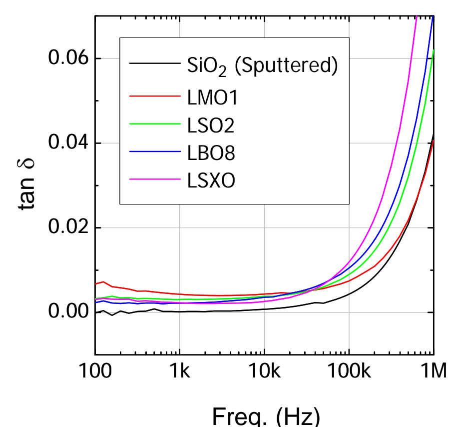

Fig.6 Frequency dependence of the dielectric loss (tanδ) for POGI films.

2-5 Fabrication and Characteristics of All-Printed Oxide TFT

In the next step, we fabricated all-printed oxide TFT arrays on a glass substrate. The gate lines for switching transistors of active matrix were solely fabricated by inkjet printing to evaluate TFT properties. The process in detail was the same in the section 2-1.

As a GI layer we selected LSXO film and it was spin coated by the same way described in the section 2-4. The thickness of the GI layer was 150 nm.

Next, SD and OSC layers were fabricated by the same way described in the section 2-2. In this section, ink-B was used for the OSC layer. Figure 7 shows photographs of the all-printed oxide TFT arrays and the inset is the expanded view of the channel region.

Figure 8 shows the I_{DS}-V_{GS} curves (Fig.8 (a)) and the histogram of the mobility for the 22 all-printed n-type doped ISO TFTs (Fig.8 (b)). The device performance of the all-printed oxide TFTs after 300 °C post-annealing exhibited the mean value in the mobility of 2.54 cm^2/Vs, the threshold voltage Vth of 7.2 V, the S-value of 0.92 V/dec, and the on/off current ratio over 10^8, respectively. Although the mobility of the TFTs is almost equal to that of the doped TFTs on Si/SiO_2 substrate in figure 4, the on-current is about three times larger because of using of the high-k gate insulator.

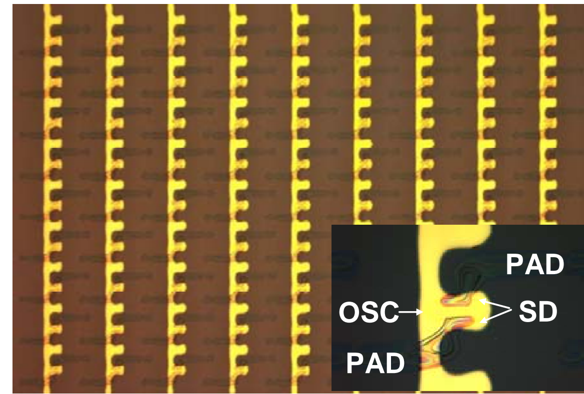

Fig.7 Photographs of all-printed oxide TFTs on a glass substrate.

This is the first report of the all-printed oxide TFT array which was patterned in the high resolution by printing technique. Moreover, small standard deviation of the mobility was obtained. This result is consistent with the case of the n-type doped TFTs fabricated on Si/SiO_2 substrate in figure 4. On the other hand, the average value of the turn-on voltage V_{ON}, at which the drain current starts to increase in the subthreshold region, was -7.19 V. The TFTs operated normally ON and the variation of the V_{ON} value was still large, these were disadvantageous characteristics as switching transistors.

Finally, figure 9 shows the case that active layer was baked at 350 °C. The TFTs exhibited the mean value in the mobility of 1.55 cm^2/Vs (Fig.9 (b)), which was a

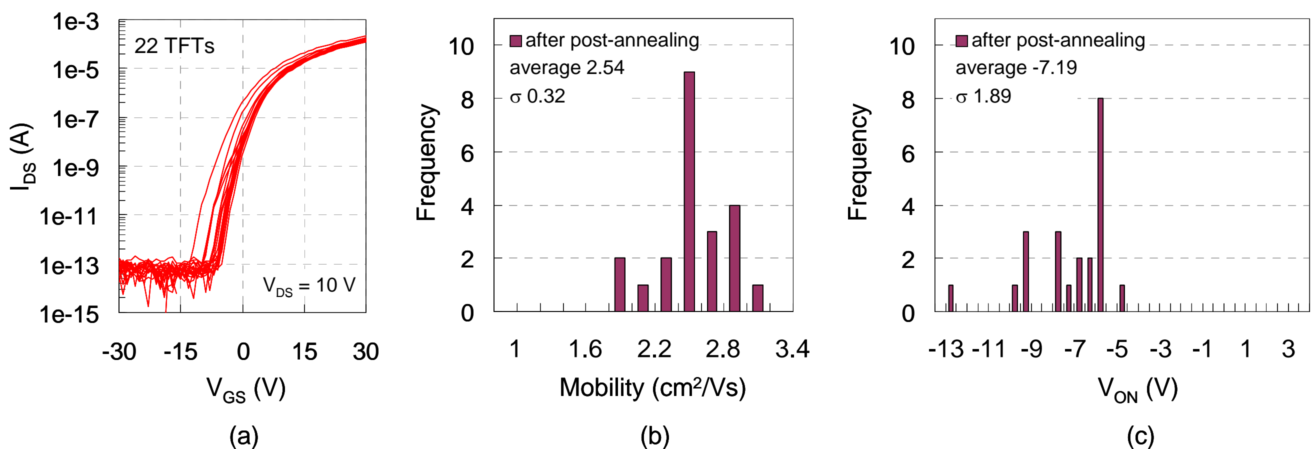

Fig.8 (a) Transfer curves after post-annealing, (b) the histogram of the mobility, (c) the histogram of the V_{ON} for 22 all-printed n-type doped ISO TFTs.

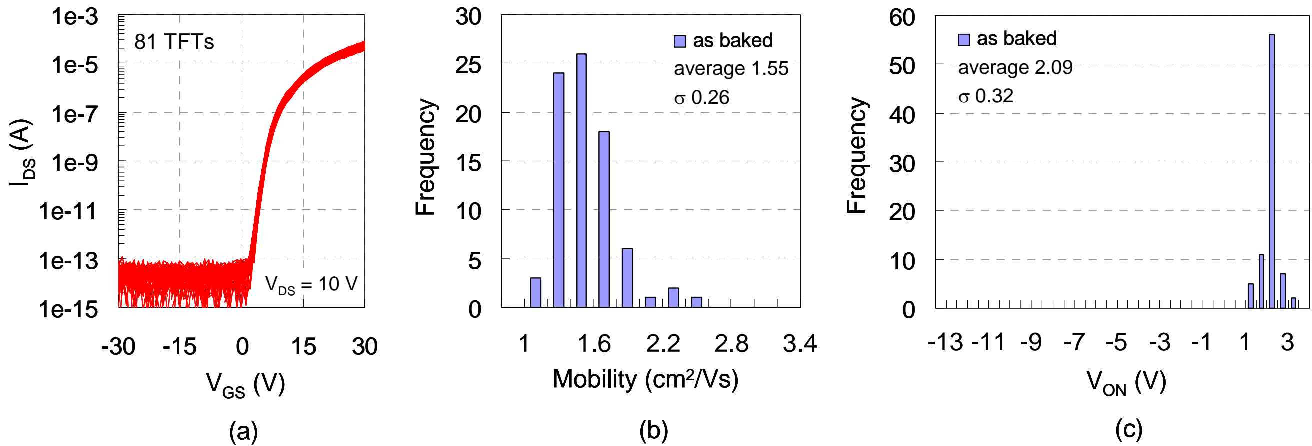

Fig.9 (a) Transfer curves as baked, (b) the histogram of the mobility, (c) the histogram of the V_{ON} for 81 all- printed n-type doped ISO TFTs.

little smaller than the 400 °C baked TFTs. But the mean value and the standard deviation of the V_{ON} were 2.09 V and 0.32 V, respectively (Fig.9 (c)). Excellent small variation of the V_{ON} value and normally-off operation were obtained. Although the detail mechanism about the difference of these results is not clear, the high performance and small variation will be satisfied all together even with the all-printed TFT.

3. Conclusion

For the first time we have developed all-printed oxide TFT arrays for 100 ppi RGB active matrix fabricated by inkjet printing and spin coating. Fine channel regions were fabricated without photolithography and mask process.

In the case of the non-doped ISO TFTs fabricated on Si/SiO_2 substrates, the average and maximum mobility after post-annealing are 7.49 and 10.49 cm^2/Vs, respectively. This is the highest device performance among the TFTs whose source-drain electrodes and the active layer were patterned by inkjet printing.

We have also shown the method of controlling the carrier generation by n-type doping to the active layer. The n-type doped TFTs exhibited the small amount of deviation in the mobility both as baked and after post-annealing. This result indicates that the method of the n-type doping to active layer has a great advantage even in the solution process; it is important for total fabrication of the active matrix backplane.

In the result of combination the novel printed high-k gate insulator and the technologies described above, the average mobility of 2.54 cm^2/Vs was achieved in all-printed oxide TFTs. Moreover, excellent small variation of TFT characteristics and normally-off operation were obtained by the all printing processes. This is the great breakthrough in the technology for all-printed oxide active matrix backplane fabrication.

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